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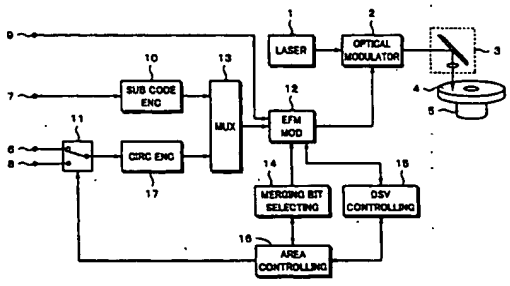
(54) DATA RECORDING MEDIUM, DATA RECORDING METHOD AND DEVICE, AND ENCODE METHOD AND DEVICE

(57) A recording method for converting m-bit data into n-bit (where n > m) data whose run length is restricted and recording the converted data on a recording medium, the recording method comprising the step of selecting first n-bit data according to an immediately preceded n-bit data, first n-bit data immediately followed thereby, and second n-bit data immediately followed thereby so that the cumulative value of DC components per unit time becomes small.

Fig. 1



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Description

Technical Field

[0001] The present invention relates to a data recording medium, a data recording method, a data recording apparatus, an encoding method, and an encoding apparatus that are applicable to for example an optical disc.

Background Art

[0002] Since optical discs such as a CD (Compact Disc) and a CD-ROM (Compact Disc Read Only Memory) are easy to handle and are produced at relatively low cost, they have been widely used as recording mediums for storing data. In recent years, a CD-R (Compact Disc Recordable) disc, on which data can be recorded once, and a CD-RW (Compact Disc ReWritable) disc, on which data can be rewritten, have come out. Thus, data can be easily recorded on such recordable optical discs. As a result, optical discs that accord with the CD standard such as a CD-DA (Compact Disc Digital Audio) disc, a CD-ROM disc, a CD-R disc, and a CD-RW disc have become the mainstream of data recording mediums. In addition, in recent years, audio data is compressed according to the MP3 (MPEG1 Audio Layer-3) and the ATRAC (Adaptive TRansform Acoustic Coding) 3 and recorded on the CD-R disc, the CD-RW disc, and so forth.

[0003] However, as a CD-R disc and a CD-RW disc have come out, data'recoded on a CD disc can be easily copied to these discs. As a result, a problem about copyright protection has arisen. Thus, when content data is recorded to a CD disc, it is necessary to take measures to protect content data.

[0004] As a conventional copy protection technology for protecting a copy of data from a CD-ROM disc to a CD-R disc or a CD-RW disc, a method for physically deforming a disc with for example wobble pits has been proposed. In the physically deforming method, however, if an original disc is a CD-R disc or a CD-RW disc, the copy protection cannot be performed.

[0005] In addition, to protect a copying operation, a method for encrypting content data has been proposed. However, even if content data has been encrypted, a disc on which the same data as an original disc is recorded can be produced.

[0006] To protect content data recorded on a CD disc that accords with the CD standard, there is a method for determining whether the disc is an original CD or a CD whose data has been copied from an original CD (this CD is referred to as copied CD). When the disc is an original CD, a copying operation thereof can be permitted. When the disc is a disc whose data has been copied from an original disc (this disc is referred to as copied disc), a further copying operation thereof can be prohibited.

[0007] To determine whether the disc is an original disc or a copied disc, a method for placing a defect on a disc in a master disc production stage, detecting the defect from the disc during a reproduction, and determining that the disc is an original disc based on the detected defect has been proposed. In this method, however, an original disc may contain such a defect. In addition, depending on the type of a defect, it may be copied as it is. Thus, content data of an original disc cannot be prevented from being copied to a CD-R disc.

[0008] Therefore, an object of the present invention is to provide a data recording medium, a data recording method, and a data recording apparatus that contribute to copy protection without need to physically deform a medium and intentionally place a defect thereon.

Disclosure of the Invention

[0009] Claim 1 of the present invention is a recording method for converting m-bit data into an n-bit (where n > m) data symbol whose run length is restricted and placing a connection bit after the m-bit data symbol so that the cumulative value of DC components per unit time becomes small, the recording method comprising the steps of selecting a first connection bit to be added to an immediately preceded data symbol from a plurality of connection bits according to at least one first connection bit that can be added between the immediately preceded data symbol and a first data symbol immediately followed thereby and according to at least one second connection bit that can be added between the first data symbol and at least one second data symbol immediately followed thereby; adding the selected first connection bit to the immediately preceded data symbol so as to generate record data; and recording the generated record data on a recording medium.

[0010] Claim 4 of the present invention is a recording method for converting m-bit data into an n-bit (where n > m) data symbol whose run length is restricted and adding a connection bit after the m-bit data symbol so that the cumulative value of DC components per unit time becomes small, the recording method comprising the steps of when an immediately preceded data symbol is a special data symbol, selecting a first connection bit to be added to the immediately preceded data symbol from a plurality of connection bits according to at least one first connection bit that can be added between the immediately preceded data symbol and a first data symbol immediately followed thereby and according to at least one second connection bit that can be added between the first data symbol and at least one second data symbol immediately followed thereby; adding the selected first connection bit to the immediately preceded data symbol so as to generate record data; and recording the generated record data on a recording medium.

[0011] Claim 9 of the present invention is a recording method for converting m-bit data into n-bit (where n > m) data whose run length is restricted and recording the

converted data on a recording medium, the recording method comprising the step of selecting first n-bit data according to an immediately preceded n-bit data, first n-bit data immediately followed thereby, and second n-bit data immediately followed thereby so that the cumulative value of DC components per unit time becomes small.

[0012] Claim 19 of the present invention is a recording apparatus, comprising an encoding process portion for performing an encoding process for input data; a converting portion for converting m-bit data that is output from the encoding processing portion into n-bit (where n > m) data whose run length is restricted by selecting first n-bit data according to an immediately preceded n-bit data, first n-bit data immediately followed thereby, and second n-bit data immediately followed thereby so that the cumulative value of DC components per unit time becomes small; and a recording portion for recording data that is output from the converting portion on a recording medium.

[0013] Claim 29 of the present invention is a recording medium on which when m-bit data is converted into n-bit (where n > m) data whose run length is restricted, first n-bit data is selected according to an immediately preceded n-bit data, first n-bit data immediately followed thereby, and second n-bit data immediately followed thereby so that the cumulative value of DC components per unit time becomes small and the selected first n-bit data is recorded after the immediately preceded n-bit data.

[0014] Claim 39 of the present invention is a data converting method, comprising the step of when m-bit data is converted into n-bit (where n > m) data whose run length is restricted, selecting first n-bit data according to an immediately preceded n-bit data, first n-bit data immediately followed thereby, and second n-bit data immediately followed thereby so that the cumulative value of DC components per unit time becomes small.

Brief Description of Drawings

[0015]

Fig. 1 is a block diagram showing an example of the structure of a mastering apparatus according to an embodiment of the present invention.

Fig. 2A and Fig. 2B are schematic diagrams showing an example of a special pattern recorded on a disc.

Fig. 3 is a schematic diagram describing the format of an EFM frame of a CD.

Fig. 4 is a schematic diagram describing a sub code block of a CD.

Fig. 5 is a schematic diagram describing Q channel of a sub code.

Fig. 6A and Fig. 6B are schematic diagrams describing data of a sub code.

Fig. 7 is a schematic diagram showing an EFM conversion table.

Fig. 8 is a schematic diagram showing an EFM conversion table.

Fig. 9 is a schematic diagram showing an EFM conversion table.

Fig. 10 is a schematic diagram showing an EFM conversion table.

Fig. 11 is a schematic diagram showing an EFM conversion table.

Fig. 12 is a schematic diagram showing an EFM conversion table.

Fig. 13A to Fig. 13D are schematic diagrams describing a method for selecting merging bits.

Fig. 14A, Fig. 14B, and Fig. 14C are schematic diagrams showing an example of a special pattern of which DSV does not converge.

Fig. 15A, Fig. 15B, and Fig. 15C are schematic diagrams showing another example of a special pattern of which DSV does not converge.

Fig. 16A, Fig. 16B, and Fig. 16C are schematic diagrams showing a further example of a special pattern of which DSV does not converge.

Fig. 17A to Fig. 17E are schematic diagrams showing an example of a special pattern of which DSV does not converge in the EFM modulation when DSV is controlled according to only the relation of an immediately preceded code symbol and a code symbol immediately followed thereby.

Fig. 18 is a schematic diagram describing an example of a special pattern of which DSV does not converge in the EFM modulation when DSV is controlled according to only the relation of an immediately preceded code symbol and a code symbol immediately followed thereby.

Fig. 19 is a flow chart describing a merging bit selecting process performed by a modulator according to the present invention.

Fig. 20A and Fig. 20B are schematic diagrams describing the merging bit selecting process performed by the modulator according to the present invention.

Fig. 21 is a block diagram showing an example of a CD reproducing apparatus.

Fig. 22 is a flow chart describing a merging bit selecting process performed by a conventional modulator.

Fig. 23A and Fig. 23B are schematic diagrams describing the merging bit selecting process performed by the conventional modulator.

Fig. 24 is a block diagram describing a flow of a disc copying process.

Fig. 25 is a block diagram showing an outline of a reproducing process portion when a disc copying process is performed.

Fig. 26 is a block diagram showing an outline of a recording process portion when a disc copying process is performed.

Best Modes for Carrying out the Invention

[0016] Next, with reference to the accompanying drawings, an embodiment of the present invention will be described. In this example, copy restriction is performed with a special pattern of which when connection bits (hereinafter referred to as merging bits) are selected in the EFM (eight to fourteen modulation) modulation, the merging bits selected when DSV (Digital Sum Variation) is controlled according to the relation of an immediately preceded code symbol and a code symbol immediately followed thereby are different from the merging bits selected in the EFM modulation when DSV is controlled according to the relation of that code symbol and a code symbol further immediately followed thereby.

[0017] Fig. 1 shows an example of the structure of a mastering apparatus that produces a data recording medium according to the present invention. A data recording medium is for example an optical disc that accords with for example the CD (Compact Disc) standard. The mastering apparatus has a laser light source 1 that is a gas laser (for example, an Ar ion laser, an He-Cd laser, or a Kr ion laser) or a semiconductor laser, an acoustooptic effect type or electrooptic type optical modulator 2 that modulates laser light emitted from the laser light source 1, and an optical pickup 3 that has an objective lens that collects laser light that has passed through the optical modulator 2 and radiates the collected light to a photoresist surface of a disc shaped glass master disc 4 on which photoresist as a photosensitive material has been coated.

[0018] The optical modulator 2 modulates the laser light emitted from the laser light source 1 corresponding to a supplied record signal. The mastering apparatus radiates the modulated laser light to the glass master disc 4. As a result, a master on which data has been recorded is produced. In addition, the mastering apparatus has a servo portion (not shown). The servo portion performs a tracking control for controlling the relative positions of the optical pickup 3 and the master disc 4 and a rotation driving operation control of a spindle motor 5. The rotations of the glass master disc 4 are driven by the spindle motor 5 at for example constant linear velocity.

[0019] The record signal is supplied from an EFM modulator 12 to the optical modulator 2. Main digital data to be recorded is supplied from an input terminal 6. The main digital data is for example two-channel stereo digital audio data. Of course, the main digital data may be still picture data, video data, or CD-ROM data as well as digital audio data. The main digital data may be also digital audio data that has been compressed according to the MP3, the ATRAC, or the like. To protect data, the main digital data may be encrypted data.

[0020] A sub code of channels P to W according to the current CD standard is supplied from an input terminal 7. A frame sync is supplied to an input terminal 9.

[0021] In addition, special pattern data is supplied from an input terminal 8. In the special pattern, merging bits selected in the EFM modulation when DSV is controlled according to the relation of an immediately preceded code symbol and a code immediately followed thereby are different from merging bits selected in the EFM modulation when DSV is controlled according to the relation of that code symbol and a code symbol further immediately followed thereby. In reality, as shown in Fig. 2A and Fig. 2B, a special pattern is a pattern of which sub code data "00h (where h represents hexadecimal notation)" or "40h" is followed by a data symbol "90h", followed by data symbols "B9h" and "9Ah" that are alternately repeated in one frame. When the sub code data "00h" and "40h" are converted according to an EFM table, code symbols (01001000100000) and (01001000100100) are obtained, respectively. The low order two bits of these code symbols are (00), which is 2T or more. The EFM conversion table will be described later. It should be noted that the foregoing pattern is just an example.

[0022] The main digital data supplied from the input terminal 6 and the special pattern data supplied from the input terminal 8 are supplied to a CIRC (Cross Interleave Reed-Solomon Code) encoder 17 through a switch circuit 11. The switch circuit 11 is switched at a predetermined timing according to an output of an area controlling circuit 16 so as to place data of the special pattern at a predetermined position of the main digital data. The CIRC encoder 17 performs an error correction code encoding process for adding error correction parity data or the like and a scrambling process. In other words, 16 bits of one sample or one word are divided into two symbols that are high order eight bits and low order eight bits. In the unit of one symbol, the error correction code encoding process for adding for example CIRC error correction parity data or the like and the scrambling process are performed.

[0023] The sub code data supplied from the input terminal 7 is converted into sub code data having the EFM frame format of a sub code by a sub code encoder 10.

[0024] An output of the CIRC encoder 17 and an output of the sub code encoder 10 are supplied to a multiplexer 13. The multiplexer 13 arranges data that is output from the CIRC encoder 17 and the sub code encoder 10 in a predetermined order. Output data of the multiplexer 13 is supplied to the EFM modulator 12. The EFM modulator 12 converts a symbol of eight bits into data of 14 channel bits according to the conversion table. A frame sync is supplied to the EFM modulator 12.

[0025] In association with the EFM modulator 12, a merging bit selecting portion 14 and a DSV controlling portion 15 are disposed. The merging bit selecting portion 14 and the DSV controlling portion 15 select merging bits (000), (001), (010), or (100) that satisfies the run length limit conditions (Tmin = 3T and Tmax = 11T) and of which DSV approaches to "0". The merging bit selecting portion 14 and the DSV controlling portion 15 perform a merging bit selecting process according to not

only the relation of an immediately preceded code symbol and a code immediately followed thereby, but also the relation of those symbols and a code symbol further immediately followed thereby that is pre-read.

[0026] An output of the EFM modulator 12 is supplied to the optical modulator 2. The EFM modulator 12 generates a record signal of the CD EFM frame format. The record signal is supplied to the optical modulator 2. With modulated laser light modulated by the optical modulator 2, photoresist on the glass master disc 4 is exposed. A developing process and an electroplating process are performed for the glass master disc 4 on which data has been recorded in such a manner. As a result, a metal master is produced. With the metal master, a mother disc is produced. With the mother disc, a stamper is produced. With the stamper, a substrate for an optical disc is produced by the compression molding method, the injection molding method, or the like. A reflection layer made of Al or the like is formed on the produced disc substrate. On the reflection layer, a protection layer is formed. As a result, an optical disc is produced.

[0027] Fig. 3 shows the data structure of one EFM frame of the CD format. In the CD format, parity Q and parity P which are four symbols each are made from a total of 12 samples (24 symbols) of two-channel digital audio data. 33 symbols (264 data bits) of which one symbol of sub code data is added to a total of 32 symbols is treated as one block. In other words, one frame which has been EFM modulated contains sub code data of one symbol, data of 24 symbols, a Q parity of four symbols, and a P parity of four symbols.

[0028] In the EFM modulating system, each data symbol (eight data bits) is converted into a code symbol of 14 channel bits. Merging bits of three bits are placed between two code symbols of 14 channel bits each. In addition, a frame sync pattern is added at the beginning of a frame. When the period of a channel bit is T, a frame sync pattern is a pattern of which 11T, 11T, and 2T are in succession. Since such a pattern does not take place according to the EFM conversion rule, a frame sync can be detected with such a special pattern. The total number of bits of one EFM frame is 588 channel bits. The frame frequency is 7.35 kHz.

[0029] As shown in Fig. 4, a block of 98 EFM frames is referred to as sub code frame (or sub code frame). A sub code frame of which 98 frames are arranged in succession is composed of a sync pattern portion that identifies the beginning of the sub code frame, a sub code portion, and a data and parity portion. A sub code frame is equivalent to 1/75 second of a reproduction time of a conventional CD.

[0030] The sub code portion is composed of 98 EFM frames. Two frames at the beginning of the sub code portion are *synchronous patterns* S0 and S1 of the sub code frame and patterns of an EFM out-of-rule. The individual bits of the sub code portion compose P, Q, R, S, T, U, V, and W channels.

[0031] Although R channel to W channel may be used for special purposes such as a still picture or a subtitle display of so-called Karaoke, they are normally not used. P channel and Q channel are used for a track position controlling operation for the pickup during reproduction of digital data recorded on the disc.

[0032] P channel is used to record a signal whose level is "0" in a so-called lead-in area, which is an inner peripheral portion of the disc and a signal whose level alternately varies between "0" and "1" at predetermined periods in a so-called lead-out area, which is an outer peripheral portion of the disc. P channel is also used to record a signal whose level is "1" between music programs in a program area formed between the lead-in area and the lead-out area of the disc and a signal whose level is "0" in the other area. P channel is used to detect the beginning of each music program during reproduction of digital audio data recorded on the CD.

[0033] Q channel is provided to more acutely control digital audio data recorded on the CD during reproduction. One sub code frame of Q channel is composed of a control bit portion, an address bit portion, a data bit portion, and a CRC (Cyclic Redundancy Check) bit portion as shown in Fig. 5.

[0034] Thus, in the program area (except for an area between music programs), as shown in Fig. 6A and Fig. 6B, a data symbol in the sub code portion is "00h" or "40h". In other words, R to W channels are not used, whereas P channel and Q channel are used. In an area between music programs, P channel is "0". When data of Q channel is "0", as shown in Fig. 6A, a data symbol in the sub code portion is "00h". When data of Q channel is "1", as shown in Fig. 6B, a data symbol in the sub code portion is "40h".

[0035] According to the present embodiment, a special pattern is placed in such a manner that merging bits selected in the EFM modulation when DSV is controlled according to the relation of an immediately preceded code symbol and a code immediately followed thereby are different from merging bits selected in the EFM modulation when DSV is controlled according to the relation of that code symbol and a code symbol further immediately followed thereby. Next, such a special pattern will be described.

[0036] As described above, in the CD format, as a modulating system used to record data, the EFM modulation is used. In the EFM modulation, eight data bits (sometimes referred to as data symbol) are converted into 14 channel bits (sometimes referred to as code symbol). In addition, when 14-bit code symbols are connected, merging bits are placed therebetween so as to satisfy the run length limit conditions and keep DC balance.

[0037] Fig. 7 to Fig. 12 show an example of the EFM conversion table that converts data bits of eight bits into channel bits of 14 bits. In Fig. 7 to Fig. 12, data symbols are represented in hexadecimal notation (00 to FF), decimal notation (0 to 255), and binary notation (d1 ..., d8). "1" of a code symbol represents that a waveform is in-

verted. The minimum time length of the EFM modulation (time length in which the number of 0s between two 1s of a record signal becomes the minimum) Tmin is 3T. The maximum time length of the EFM modulation (time length in which the number of 0s between two 1s of a record signal becomes the maximum) Tmax is 11T. The pit length equivalent to T is the shortest pit length. All code symbols shown in Fig. 7 to Fig. 12 satisfy rules of which the minimum time length is 3T and the maximum time length Tmax is 11T (hereinafter they are referred to as run length limit conditions).

[0038] Between two code symbols of 14 bits each, three merging bits are placed so as to satisfy the foregoing run length limit conditions and keep the DC balance. As merging bits, there are four types of patterns "000", "001", "010", and "100". Among the four patterns of merging bits, one pattern that satisfies the run length limit conditions of which the minimum time length Tmin is 3T and the maximum time length is 11T and of which DSV (Digital Sum Variation) is close to "0" is selected.

[0039] Next, an example of which merging bits are used to connect code symbols of 14 bits each will be described with reference to Fig. 13A to Fig. 13D. The following example is described in "Book on Compact Disc (Version 3) [translated title; written in Japanese]", published by Ohm-Sha Publishing Company, Japan, March 25, 2001.

[0040] As shown in Fig. 13A, the cast that a preceded pattern of 14 bits ends with "010" and a data symbol immediately followed thereby is "01110111" ("77h" in hexadecimal notation and "119" in decimal notation) will be considered. The data symbol is converted into a code symbol of 14 bits (00100010000010) according to the conversion table shown in Fig. 7 to Fig 12. In Fig. 13A to Fig. 13D, before timing t0, the code symbol of 14 bits ends. At timing t_1 after the period of merging bits, the immediately followed code symbol of 14 bits starts. At timing t_2, the further followed pattern of 14 bits starts. The waveform is inverted at "1".

[0041] When the preceded pattern of 14 bits ends with (010) and the immediately followed code symbol of 14 bits is converted into (*00100010000010*), if the merging bits (100) of the foregoing four patterns are used, the condition of Tmin = 3T is not satisfied. Thus, the merging bits (100) cannot be used. From the rest of patterns of the merging bits (000), (010), and (001), one pattern that decrease DSV is selected.

[0042] DSV is a cumulative value of which when a waveform is in a high level, "+1" is counted and when a waveform is in a low level, "-1" is counted. As an example, it is assumed that DSV at timing t0 is (-3).

[0043] Fig. 13B shows the case that "000" are used as merging bits. Fig. 13C shows the case that "010" are used as merging bits. Fig. 13D shows the case that "001" are used as merging bits.

[0044] As shown in Fig. 13B, when (000) are used as merging bits, DSV is "-3" at timing t0. DSV is "+3" in period (t0 to t1). DSV is "+2" (+2 - 4 + 6 - 2 = +2) in period (t1 to t2). Thus, DSV is (-3 + 3 + 2 = +2) at timing t2.

[0045] As shown in Fig. 13C, when (010) are used as merging bits, DSV is "-3" at timing t0. DSV is "-1" (+1 - 2 = -1) in period (t0 to t1). DSV is "-2" (-2 + 4 - 6 + 2 = -2) in period (t1 to t2). Thus, DSV is (-3 - 1 - 2 = -2) at timing t2.

[0046] As shown in Fig. 13D, when (001) are used as merging bits, DSV is "-3" at timing t0. DSV is "+1" (+2 - 1 = 1) in period (t0 to t1). DSV is "-2" (-2 + 4 - 6 + 2 = -2) in period (t1 to t2). Thus, DSV is (-3 + 1 - 2 = -4) at timing t2.

[0047] Thus, when the preceded pattern of 14 bits ends with (010) and the immediately followed code symbol of 14 bits is converted into (00100010000010), merging bits that satisfy the run length limit conditions (Tmin = 3T and Tmax = 11T) are (000), (010), and (001). When (000) are used as merging bits, DSV becomes "+2". When (010) are used as merging bits, DSV becomes "-6". When (001) are used as merging bits, DSV becomes "-4". Thus, merging bits (000) of which DSV becomes closest to "0" at timing t2 are selected as merging bits in period (t0 to t1).

[0048] Thus, when code symbols of 14 bits each are connected, merging bits are selected from four patterns of (000), (001), (010), and (100) that satisfy the rules (Tmin = 3T and Tmax = 11T) and of which the cumulative value of DSV approaches to "0". As a result, the run length limit conditions (Tmin = 3T and Tmax = 11T) can be satisfied. In addition, DSV converges to "0". In such a manner, in the EFM, when merging bits are properly selected, DSV can be caused to converge to "0". When DSV converges to "0", the DC balance is kept. When the DC balance is not kept, the slice level in which data is reproduced goes wrong. As a result, an error increases and the spindle servo gets disordered. Substantially, the reproducing operation cannot be performed.

[0049] However, even if merging bits are selected, DSV does not always converge to "0" in every pattern. In other words, in some special patterns, DSV does not converge to "0".

[0050] For example, a pattern of which data symbols "FAh" are repeated as shown in Fig. 14A is considered. When a data symbol "FAh" is converted into a code symbol of 14 bits according to the foregoing conversion table, a code symbol (10010000010010) is obtained. As merging bits that connect code symbols (10010000010010), into which data symbols "FAh" have been converted, as shown in Fig. 14B, (000) are unconditionally used. This is because other merging bits ((001), (010), and (100)) do not satisfy the run length limit condition Tmin = 3T.

[0051] Fig. 14C shows a waveform of the pattern shown in Fig. 14B. As is clear from Fig. 14C, in the pattern, DSV negatively increases by "-5" (-3 + 3 - 6 + 3 - 2 = -5) in period (t10 to f11). Thus, in a pattern of which data symbols "FAh" are repeated, DSV negatively increases, not converges to "0".

[0052] Next, a pattern of which data symbols "FBh"

are repeated as shown in Fig. 15A is considered. When a data symbol "FBh" is converted into a code symbol of 14 bits according to the foregoing conversion table, a code symbol (10001000010010) is obtained. As merging bits that connect code symbols (10001000010010), into which data symbols "FBh" have been converted, due to the run length limit conditions (Tmin = 3T and Tmax = 11T), (000) are unconditionally selected as shown in Fig. 15B.

[0053] Fig. 15C shows a waveform of the pattern shown in Fig. 15B. As is clear from Fig. 15C, when code symbols (10001000010010) of 14 channel bits each, into which data symbols "FBh" have been converted, are connected with merging bits (000), DSV negatively increases by (-3 + 4 - 5 + 3 - 2 = -3) in period (t20 to t21). Thus, in a pattern of which data symbols "FBh" are repeated, DSV negatively increases, not converges to "0".

[0054] As shown in Fig. 16A, a pattern of which data symbols "FAh" and "FBh" are alternately repeated. When a data symbol "FAh" is converted into a code symbol of 14 bits according to the foregoing conversion table, a code symbol (10010000010010) is obtained. When a data symbol "FBh" is converted into a code symbol of 14 bits according to the foregoing conversion table, a code symbol (10001000010010) is obtained. As merging bits that connect the code symbol (10010000010010), into which the data symbol "FAh" has been converted, and the code symbol (10001000010010), into which the data symbol "FBh" has been converted, due to the run length limit condition (Tmin = 3T), (000) are unconditionally selected as shown in Fig. 16B.

[0055] Fig. 16C shows a waveform of the pattern shown in Fig 16B. As is clear from Fig. 16C, when the code symbol (10010000010010), into which the data symbol "FAh" has been converted, and the code symbol (10001000010010), into which the data symbol "FBh" has been converted, are connected with the merging bits (000), as the waveform shown in Fig. 16C, DSV negatively increases by "-5" (-3 + 3 - 6 + 3 - 2 = -5) in period (t30 to t31). DSV negatively increases by "-3" (-3 + 4 - 5 + 3 - 2 = -3) in period (t31 to t32). Thus, in a pattern of which "FAh" and "FBh" are alternately repeated, DSV negatively increases, not converges to "0".

[0056] Thus, in the foregoing special patterns, merging bits cannot be selected. Consequently, using flexibility of merging bits, the function for causing DSV to converge to "0" does not work. As long as such a data pattern continues, DSV positively or negatively continues to increase. Unless DSV converges to "0", the DC balance is lost, an error increases, and the servo gets disordered. Substantially, the reproducing operation for the disc cannot be performed.

[0057] It is clear that special patterns of which DSV does not converge to "0" are not limited to the foregoing examples. For example, when a converted code symbol of 14 bits that ends with "0T" or "1T" and a converted code symbol of 14 bits that begins with "0T" or "1T" are connected, merging bits cannot be selected. Thus, there is a possibility of which DSV does not converge to "0".

[0058] As described above, as merging bits that connect code symbols of 14 bits each, merging bits are selected from (000), (100), (010), and (001) that satisfy the run length limit conditions (Tmin = 3T and Tmax = 11T) and of which DSV approaches to "0". Merging bits are selected so that they satisfy the run length limit conditions (Tmin = 3T and Tmax = 11T) and the cumulative value of DSV approaches to "0".

[0059] However, there is a special pattern of which when merging bits are selected according to the relation of an immediately preceded code symbol and a code symbol immediately followed thereby so that DSV approaches to "0", DSV increases according to the relation of those code symbol and a code symbol further immediately followed thereby. In other words, there is a special pattern of which merging bits selected in the EFM modulation when DSV is controlled according to the relation of an immediately preceded code symbol and a code symbol immediately followed thereby is different from merging bits selected in the EFM modulation when DSV is controlled according to the relation of those symbols and a code symbol further immediately followed thereby. In such a special pattern, it is necessary to select merging bits according to not only the relation of an immediately preceded code symbol and a code symbol immediately followed thereby, but also the relation of those code symbol and a code symbol further immediately followed thereby.

[0060] Next, a pattern of which a data symbol "90h" is followed by data symbols "B9h" and "9Ah" that are alternately repeated is considered.

[0061] When a data symbol "90h" is converted into a code symbol of 14 bits according to the foregoing conversion table, a code symbol of 14 bits (10000000100001) is obtained. When the immediately preceded code symbol ends with "00", (the sub code is "00h" or "40h" and the code symbol thereof ends with "00"), merging bits that immediately precede the code data (10000000100001) are (000) or (100) due to the run length limit conditions (Tmin = 3T and Tmax = 11T). The merging bits (000) or (100) are selected depending on DSV. Fig. 17B and Fig. 17C show the case that merging bits (000) have been selected. Fig. 17D and Fig. 17E show the case that (100) are selected as merging bits.

[0062] In Fig. 17A to Fig. 17E, it is assumed that the cumulative value of DSV is (-50) until timing t50. As shown in Fig. 17B, when (000) are selected as merging bits. DSV varies by "+1" (-3 + 8 - 5 + 1 = +1) in period (t50 to t51). DSV is (-49) at timing t51.

[0063] In contrast, as shown in Fig. 17D, when (100) are selected as merging bits, DSV varies by "-1" (+3 -8 + 5 - 1 = -1) in period (t50 to t51). DSV is "-51" at timing t51.

[0064] Thus, when (000) are selected as merging bits, DSV is "-49" at timing t51. When (100) are selected as merging bits, DSV is "-51" at timing t51. Thus, normally,

(000) are selected as merging bits.

[0065] However, in such a pattern, when (000) are selected as merging bits, as denoted by broken line L1 of Fig. 18, DSV negatively increases. Thus, DSV does not converge to "0". On the other hand, when (100) are selected as merging bits, as denoted by broken line L2 of Fig. 18, DSV converges to "0".

[0066] In other words, when (000) are selected as merging bits, thereafter, the waveform varies as shown in Fig. 17C.

[0067] As shown in Fig. 17A to Fig. 17E, a data symbol "90h" is followed by a data symbol "B9h". When the data symbol "B9h" is converted into a code symbol of 14 bits according to the foregoing conversion table, a code symbol "10000000001001" is obtained. As merging bits placed between the code data (10000000100001), into which the data symbol "90h" has been converted, and the code data (10000000001001), into which the data symbol "B9h" has been converted, due to the run length limit conditions (Tmin = 3T and Tmax = 11T), merging bits (000) are unconditionally selected. When (000) are selected as merging bits, DSV varies by "-5" (+3 -10 + 3 - 5 = -5) in period (t51 to t52). DSV is "-54" at timing t52.

[0068] The data symbol "B9h" is followed by a data symbol "9Ah". When the data symbol "9Ah" is converted into a code symbol of 14 bits according to the foregoing code symbol, a code symbol (10010000000001) is obtained. As merging bits placed between the code data (10000000001001), into which the data symbol "B9h" has been converted, and the code symbol (10010000000001), into which the data symbol "9Ah" has been converted, due to the run length limit conditions (Tmin = 3T and Tmax = 11T), (000) are unconditionally selected. When (000) are selected as merging bits, DSV varies by "-9" (-3 + 3 - 10 + 1 = -9) in period (t52 to t53). DSV is "-63" at timing t53.

[0069] Thereafter, DSV varies by "-5" in the period of the data symbol "B9h". DSV varies by "-9" in the period of the data symbol "9Ah". DSV varies as denoted by broken line L1 of Fig. 18. Thereafter, since the data symbols "9Ah" and "B9h" are alternately repeated, DSV negatively increases. Thus, DSV does not converge to "0".

[0070] In contrast, Fig. 17E shows a waveform in the case that (100) are selected as the first merging bits.

[0071] As shown in Fig. 17A to Fig. 17E, the data symbol "90h" is followed by the data symbol "B9h". When the data symbol "B9h" is converted into a code symbol of 14 bits, a code symbol (10000000001001) is obtained. As merging bits placed between the code data (10000000100001), into which the data symbol "90h" has been converted, and the code data (10000000001001), into which the data symbol "B9h" has been converted, due to the run length limit conditions (Tmin = 3T and Tmax = 11T), (000) are unconditionally selected. When (000) are selected as merging bits, DSV varies by "+5" (-3 + 10 - 3 + 1 = +5) in period (t51 to t52). DSV is "-46" at timing t52.

[0072] The data symbol "B9h" is followed by the data symbol "9Ah". When the data symbol "9Ah" is converted into a code symbol of 14 bits, a code symbol (10010000000001) is obtained. As merging bits placed between the code data (10000000001001), into which the data symbol "B9h" has been converted, and the code data (10010000000001), into which the data symbol "9Ah" has been converted, due to the run length limit conditions (Tmin = 3T and Tmax = 11T), (000) are unconditionally selected. When (000) are selected as the merging bits, DSV varies by "+9" (+3 - 3 + 10 - 1 = +9) in period (t52 to t53). DSV is "-37" at timing t53.

[0073] Thereafter, DSV varies by "+5" in the period of the data symbol "B9h". DSV varies by "+9" in the period of the data symbol "9Ah". DSV varies as denoted by broken line L2 of Fig. 18. Thus, thereafter, the data symbol "9Ah" and the data symbol "B9h" are alternately repeated. As a result, DSV positively increases. As denoted by broken line L2 of Fig. 18, DSV converges to "0".

[0074] In such a special pattern, when merging bits are selected so that DSV approaches to "0" according to the relation of an immediately preceded code symbol and a code symbol immediately followed thereby, thereafter, DSV positively or negatively increases. In such a pattern, it is necessary to select merging bits according to not only the relation of an immediately preceded code symbol and a code symbol immediately followed thereby, but also the relation of that code symbol and a code symbol further immediately followed thereby. Such a pattern is not limited to the foregoing example.

[0075] In the foregoing example, merging bits of which DSV approaches to "0" according to the relation of an immediately preceded code symbol and a code symbol immediately followed thereby are different from merging bits of which DSV approaches to "0" according to the relation of that code symbol and a code symbol further immediately followed thereby. However, according to the present invention, a special pattern of which merging bits or a conversion pattern selected when DSV is calculated according to the relation of one code symbol and A code symbols immediately followed thereby is different from merging bits or a conversion pattern selected when DSV is calculated according to the relation of one code symbol and B (where B > A) code symbols immediately followed thereby can be used. The predetermined number A is normally "1".

[0076] As described above, in the EFM modulation, using the flexibility of merging bits, DSV is caused to converge to "0". However, it is clear that in a special pattern merging bits are unconditionally selected and DSV cannot be caused to converge to "0".

[0077] It is clear that in a special pattern merging bits selected in the EFM modulation when DSV is controlled according to the relation of an immediately preceded code symbol and a code symbol immediately followed thereby are different from merging bits selected in the EFM modulation when DSV is controlled according to the relation of that code symbol and a code symbol fur-

ther immediately followed thereby.

[0078] In the case that such a special pattern is contained in an original disc, when data is reproduced from the original disc, the reproduced data is encoded by a conventional encoder, and the encoded data is recorded on a recording medium such as a CD-R disc, then a recording medium of which DSV does not converge to "0" is produced. As a result, the reproduced data would not been correctly read from the medium.

[0079] In the example, as described above, a special pattern of which merging bits selected in the EFM modulation when DSV is controlled according to the relation of an immediately preceded code symbol and a code symbol immediately followed thereby are different from merging bits selected in the EFM modulation when DSV is controlled according to the relation of that code symbol and a code symbol further immediately followed thereby is used.

[0080] In other words, in the master apparatus shown in Fig. 1, which produces an original CD, the EFM modulator 12, the merging bit selecting portion 14, and the DSV controlling portion 15 select merging bits according to not only the relation of an immediately preceded code symbol and a code symbol immediately followed thereby, but also the relation of that code symbol and a code symbol further immediately followed thereby that is pre-read. Thus, even if an original recording medium produced by the master apparatus contains a special pattern shown in Fig. 2A, Fig. 2B, or Fig. 17A to Fig. 17E, merging bits are selected so that DSV converges to "0". In contrast, when data of an original recording medium is copied to a CD-R disc or the like, the EFM modulating portion selects merging bits of which DSV approaches to "0" according to the relation of only an immediately preceded code symbol and a code symbol immediately followed thereby not the relation of that code symbol and a code symbol further immediately followed thereby that is pre-read. Thus, when a special pattern shown in Fig. 2A, Fig. 2B, or Fig. 17A to Fig. 17E is reproduced from a copied recording medium, since DSV increases, the reproducing operation cannot be performed.

[0081] Fig. 19 is a flow chart showing an example of a process for selecting merging bits according to not only the relation of an immediately preceded code symbol and a code symbol immediately followed thereby, but also the relation of that code symbol and a code symbol further immediately followed thereby that is pre-read as with the EFM modulator 12, the merging bit selecting portion 14, and the DSV controlling portion 15 of the mastering apparatus shown in Fig. 1.

[0082] As shown in Fig. 20A, an immediately preceded data symbol of eight bits is denoted by D0, a current data symbol of eight bits is denoted by D1, a data symbol of eight bits immediately followed thereby is denoted by D2, and data symbols further immediately followed thereby are denoted by D3, D4, ..., and so forth.

[0083] As shown in Fig. 20B, these data symbols D0, D1, D2, D3, D4, ... and so forth are converted into code symbols of 14 bits each. The converted code symbols are denoted by d0, d1, d2, d3, ..., and so forth. The position of merging bits placed between the code symbol d0 and the code symbol d1 is denoted by (A = 1). The position of merging bits placed between the code symbol d1 and the code symbol d2 is denoted by (A = 2). Alternatives of four patterns of merging bits of (A = 1) are denoted by MPn (1) ((MP0 (1) = 000), (MP1 (1) - 001), (MP2 (1) = 010), and (MP3 (1) = 100). Alternatives of four patterns of merging bits of (A = 2) are denoted by MPn (2) ((MP0 (2) = 000), (MP1 (2) = 001), (MP2 (2) = 010), and (MP3 (2) = 100)).

[0084] In Fig. 19, when merging bits placed between the code symbol d0 and the code symbol d1 immediately followed thereby are selected, the data symbol D1 of eight bits and the data symbol D2 immediately followed thereby are input (at step S1). The data symbols D1 and D2 are converted into code symbols d1 and d2 of 14 bits each according to the conversion table (at step S22). Alternative merging bits placed between the code symbol d0 and the code symbol d1 (A1) and alternative merging bits placed between the code symbol d1 and the code symbol d2 (A2) are selected (at step S3).

[0085] First of all, (A = 1), (n (1) = 0) are set. With merging bits MP0 (1) (MP0 (1) = 000), the code symbol d0 and the code symbol d1 (at position A = 1) are tried to be connected (at step S4). With the merging bits MP0 (1), the code symbol d0 and the code symbol d1 are tried to be connected and it is determined whether or not the run length limit condition of the minimum inversion period (Tmin = 3T) is satisfied (at step S5). When the condition of the minimum inversion period (Tmin = 3T) is satisfied, it is determined whether or not the run length limit condition of the maximum inversion period (Tmax = 11T) is satisfied (at step S6).

[0086] When the condition of the minimum inversion period (Tmin = 3T) is not satisfied at step S5 or when the condition of the maximum inversion period (Tmax = 11T) is not satisfied at step S6, n (1) is incremented (at step S7). With the merging bits MPn + 1 (1), the code symbol d0 and the code symbol d1 are tried to be connected (A = 1) and it is determined whether or not the run length limit condition of the minimum inversion period (Tmin = 3T) is satisfied (at step S5). When the condition of the minimum inversion period (Tmin = 3T) is satisfied, it is determined whether or not the run length limit condition of the maximum inversion period (Tmax = 11T) is satisfied (at step S6).

[0087] When the condition of the minimum inversion period (Tmin = 3T) is satisfied at step S5 and when the condition of the maximum inversion period (Tmax = 11T) is satisfied at step S6, as merging bits that satisfy the run length limit conditions of (A = 1), the information is stored (at step S8). Thereafter, it is determined whether or not (n (1) = 3) is satisfied (at step S9). When (n (1) = 3) is not satisfied, n (1) is incremented (at step S7). With the merging bits MPn + 1 (1), the code symbol d0 and the code symbol d1 are tried to be connected (A = 1)

and it is determined whether or not the run length limit condition of the minimum inversion period (Tmin = 3T) is satisfied (at step S5). When the condition of the minimum inversion period (Tmin = 3T) is satisfied, it is determined whether or not the run length limit condition of the maximum inversion period (Tmax = 11T) is satisfied (at step S6).

[0088] By repeating the foregoing process, with the merging bits MP0 (1) (MP0 (1) = 000), MP1 (1) (MP1 (1) = 001), MP2 (1) (MP2 (1) = 010), MP3 (1) (MP3 (1) = 100), the code symbol d0 and the code symbol d1 are connected (A = 1) and it is determined whether or not the run length limit conditions of the minimum inversion period (Tmin = 3T) and the maximum inversion period (Tmax = 11T) are satisfied. The information of merging bits that satisfy the run length limit conditions is stored at step S8.

[0089] When the determined result at step S9 represents that (n (1) = 3) is satisfied, it is determined whether or not (A = 2) is satisfied (at step S10). When (A = 2) is not satisfied, A is incremented (at step S11). Thereafter, the flow returns to step S5.

[0090] Thereafter, (A = 2), (n (2) = 0) are set. With the merging bits MP0 (2) (MP0 (2) = 000), the code symbol d1 and the code symbol d2 are tried to be connected (A = 2). With the merging bits MP0 (2), the code symbol d1 and the code symbol d2 are tired to be connected and it is determined whether or not the run length limit condition of the minimum inversion period (Tmin = 3T) is satisfied (at step S5). When the condition of the minimum inversion period (Tmin = 3T) is satisfied, it is determined whether or not the run length limit condition of the maximum inversion period (Tmax = 11T) is satisfied (at step S6).

[0091] When the condition of the minimum inversion period (Tmin = 3T) is not satisfied at step S5 or when the condition of the maximum inversion period (Tmax = 11T) is not satisfied at step S6, n (2) is incremented (at step S7). With the merging bits Mpn + 1 (2), the code symbol d1 and the code symbol d2 are tired to be connected (A = 2) and it is determined whether or not the run length limit conditions of the minimum inversion period (Tmin = 3T) is stratified (at step S5). When the condition of the minimum inversion period (Tmin = 3T) is satisfied, it is determined whether or not the run length limit condition of the maximum inversion period (Tmax = 11T) is satisfied (at step S6).

[0092] When the condition of the minimum inversion period (Tmin = 3T) is satisfied at step S5 and when the condition of the maximum inversion period (Tmax = 11T) is satisfied at step S6, as merging bits that satisfy the run length limit conditions of (A = 2), this information is stored (at step S8). Thereafter, it is determined whether or not (n (2) = 3) is satisfied (at step S9). When (n (2) = 3) is not satisfied, n (2) is incremented (at step S7). With the merging bits MPn + 1 (2), the code symbol d1 and the code symbol d2 are tired to be connected (A = 2) and it is determined whether or not the run length limit condition of the minimum inversion period (Tmin = 3T) is satisfied (at step S5). When the condition of the minimum inversion period (Tmin = 3T) is satisfied, it is determined whether or not the run length limit condition of the maximum inversion period (Tmax = 11T) is satisfied (at step S6).

[0093] By repeating the foregoing process, with the merging bits MP0 (2) (MP0(2) = 000), MP1 (2) (MP1 (2) = 001), MP2 (2) (MP2 (2) = 010), MP3 (2) (MP3 (2) = 100), the code symbol d1 and the code symbol d2 are connected (A = 2) and it is determined whether or not the run length limit conditions of the minimum inversion period (Tmin = 3T) and the maximum inversion period (Tmax = 11T) are satisfied. The information of the merging bits that satisfy the run length conditions is stored at step S8.

[0094] When the determined result at step S9 represents that (n (2) = 3) is satisfied, it is determined whether or not (A = 2) is satisfied (at step S9). When (A = 2) is satisfied, with a combination of the merging bit information that satisfies the run length limit conditions of the minimum inversion period (Tmin = 3T) and the maximum inversion period (Tmax = 11T) at the position (A = 1) stored at step S8 and the merging bit information that satisfies the run length limit conditions of the minimum inversion period (Tmin = 3T) and the maximum inversion period (Tmax = 11T), DSV is calculated. In other words, in a combination of the merging bits MPn (1) that satisfy the conditions and that are placed between the immediately preceded code symbol d0 and the current code symbol d1 (A = 1) and the merging bits MPn (2) that satisfy the conditions and that are placed between the current code symbol d1 and the code symbol d2 immediately followed thereby (A = 2), DSV is obtained. In the combination, the minimum value of the absolute values of DSV is selected (at step S12). Thus, merging bits placed between the code symbol d0 and the current code symbol d1 (A = 1) are decided (at step S13).

[0095] In the example, merging bits placed between the code symbol d0 and the code symbol d1 immediately followed thereby (A = 1) are decided by pre-reading the code symbol D2 further immediately followed thereby, converting the code symbol D2 into the code symbol d2, and considering merging bits selected between the code symbol d1 and the code symbol d2 (A = 2). In addition, to decide the merging bits, the data symbols D3, D4, ... and so forth may be pre-read.

[0096] Fig. 21 shows an example of the structure of a reproducing apparatus that reproduces data from an optical disc that has been produced in the foregoing mastering and stamping processes.

[0097] Although the structure of the reproducing apparatus is the same as that of a conventional player or drive, the structure will be described for easy understanding of the present invention. In Fig. 21, reference numeral 21 represents a disc as a recording medium produced in the foregoing mastering and stamping processes. Reference numeral 22 represents a spindle mo-

tor that drives the rotations of the disc 21. Reference numeral 23 represents an optical pickup that reproduces a signal from the disc 21. The optical pickup 23 is composed of a semiconductor laser that radiates laser light to the disc 21, an optical system such as an objective lens, a detector that receives light reflected from the disc 21, a focus and tracking mechanism, and so forth. The optical pickup 23 is traveled in the radius direction of the disc 21 by a thread mechanism (not shown).

[0098] Output signals of for example a four-divided detector of the optical pickup 23 are supplied to an RF portion 24. The RF portion 24 calculates the output signals of the individual detector elements of the four-divided detector and generates a reproduction (RF) signal, a focus error signal, and a tracking error signal. The reproduction signal is supplied to a sync detecting portion 25. The sync detecting portion 25 detects a frame sync from the beginning of each EFM frame. The detected frame sync, the focus error signal, and the tracking error signal are supplied to a servo portion 26. The servo portion 26 controls the rotations of the spindle motor 22 and performs a focus servo and a tracking servo of the optical pickup 23 corresponding to a reproduced clock of the RF signal.

[0099] Main data that is output from the sync detecting portion 25 is supplied to an EFM demodulator 27. The EFM demodulator 27 performs an EFM demodulating process for the main data. Main digital data is supplied from the EFM demodulator 27 to a CIRC decoder 28. The CIRC decoder 28 performs an error correcting process for the main digital data. An interpolating circuit 29 interpolates the main digital data and outputs the interpolated data as reproduced data to an output terminal 30. Sub code data is supplied from the EFM demodulator 27 to a system controller 32.

[0100] The system controller 32 is composed of a microcomputer. The system controller 32 controls operations of the whole reproducing apparatus. In association with the system controller 32, an operation button and display portion 33 is disposed. The system controller 32 controls the servo portion 26 so as to access a desired position of the digital 21.

[0101] According to the present embodiment, as described above, a special pattern of which merging bits selected in the EFM modulation when DSV is controlled according to the relation of an immediately preceded code symbol and a code symbol immediately followed thereby are different from merging bits selected in the EFM modulation when DSV is controlled according to the relation of that code symbol and a code symbol further immediately followed thereby is recorded on the disc 21. The EFM modulator 12 of the master apparatus shown in Fig. 1 has the merging bit selecting portion 14 and the DSV controlling portion 15. As shown in Fig. 19, the merging bit selecting portion 14 and the DSV controlling portion 15 perform the merging bit selecting process according to not only the relation of an immediately preceded code symbol and a code symbol immediately followed thereby, but also the relation of those code symbol and a code symbol further immediately followed thereby that is pre-read. Thus, in such a special pattern, merging bits are added so that DSV finally converges to "0". Thus, when an original disc 21 is used, the special pattern portion can be reproduced.

[0102] However, a conventional CD-R disc recording apparatus selects merging bits of which DSV approaches to "0" in the EFM modulation according to the relation of an immediately preceded code symbol and a code symbol immediately followed thereby. Thus, when data is copied from the original disc 21, in the special pattern of the copied disc, DSV does not converge to "0". As a result, the DC balance is lost and the reproducing operation cannot be performed. Consequently, the copying operation can be prevented.

[0103] Fig. 22 is a flow chart showing a merging bit controlling process performed by a conventional EFM modulator disposed in a CD-R disc drive and a CD-RW disc drive.

[0104] As shown in Fig. 23A, an immediately preceded data symbol is denoted by D0, a data symbol of eight bits immediately followed thereby is denoted by D1, a data symbol of eight bits further immediately followed thereby is denoted by D2, and other data symbols further immediately followed thereby are denoted by D3, D4, ... and so forth.

[0105] As shown in Fig. 23B, these code symbols D0, D1, D2, D3, D4, ... and so forth are converted into code symbols of 14 bits. These converted code symbols are denoted by d1, d2, d3, ... and so forth. Alternatives of four patterns of merging bits placed between the code symbol d0 and the code symbol d1 are denoted by MPn ((MP0 = 000), MP1 (MP1 = 001), MP2 (MP2 = 010), and MP3 (MP3 = 100).

[0106] In Fig. 22, when merging bits placed between the code symbol d0 and the code symbol d1 immediately followed thereby are selected, the data symbol D1 of eight bits is input (at step S51). The data symbol D1 is converted into the code symbol d1 of 14 bits according to the conversion table (at step S52). Thereafter, merging bits placed between the current code symbol d1 and the code symbol d0 immediately preceded thereby are selected (at step S53).

[0107] At first, n = 0 is set (at step S54). With the merging bits MP0 (MP0 = 000), the immediately preceded code symbol d0 and the current code symbol d1 are tried to be connected (at step S54). With the merging bits MP0, the immediately preceded code symbol d0 and the current code symbol d1 are tried to be connected and it is determined whether or not the run length limit condition of the minimum inversion period (Tmin = 3T) is satisfied (at step S55). When the condition of the minimum inversion period (Tmin = 3T) is satisfied, it is determined whether or not the run length limit condition of the maximum inversion period (Tmax = 11T) is satisfied (at step S56).

[0108] When the condition of the minimum inversion

period (Tmin = 3T) is not satisfied at step S55 or when the condition of the maximum inversion period (Tmax = 11T) is not satisfied at step S56, n is incremented (at step S57). With the merging bits MPn + 1, the immediately preceded code symbol d0 and the current code symbol d1 are tried to be connected and it is determined whether or not the run length limit condition of the minimum inversion period (Tmin = 3T) is satisfied (at step S55). When the condition of the minimum inversion period (Tmin = 3T) is satisfied, it is determined whether or not the run length limit condition of the maximum inversion period (Tmax = 11T) is satisfied (at step S56).

[0109] When the condition of the minimum inversion period (Tmin = 3T) is satisfied at step S55 and when the condition of the maximum inversion period (Tmax = 11T) is satisfied at step 556, as merging bits that satisfy the run length limit conditions, the information is stored (at step S58). Thereafter, it is determined whether or not (n = 3) is satisfied (at step S59). When (n = 3) is not satisfied, n is incremented (at step S57). With the next merging bits MPn + 1, the immediately preceded code symbol d0 and the current code symbol d1 are tried to be connected and it is determined whether or not the run length limit condition of the minimum inversion period (Tmin = 3T) is satisfied (at step S55). When the condition of the minimum inversion period (Tmin = 3T) is satisfied, it is determined whether or not the run length limit condition of the maximum inversion period (Tmax = 11T) is satisfied (at step S56).

[0110] By repeating the foregoing process, n advances from "0" to "3". With the merging bits MP0 (MP0 = 000), MP1 (MP1 = 001), MP2 (MP2 = 010), and MP3 (MP3 = 100), the code symbol d0 and the code symbol d1 are connected and it is determined whether or not the run length limit conditions of the minimum inversion period (Tmin = 3T) and the maximum inversion period (Tmax = 11T) are satisfied. Information of merging bits that satisfy the run length limit conditions is stored at step 558.

[0111] When the determined result at step S59 represents that (n = 3) is satisfied, with the merging bits MPn that satisfy the conditions, DSV is calculated. In other words, according to the information stored at step S58, with alternative merging bits MPn that satisfy the conditions and that are placed between the code symbol d0 and the code symbol d1, DSV is obtained. The minimum value of absolute values of DSV is selected (at step S60). Thus, merging bits placed between the code symbol d0 and the code symbol d1 are decided (at step S61).

[0112] In the process shown in Fig. 22, merging bits placed between the code symbol d0 and the code symbol d1 are selected according to only the relation of the immediately preceded code symbol d0 and the current code symbol d1. In this case, when a special pattern shown in Fig. 2A, Fig. 2B, or Fig. 17A to Fig. 17E is contained, since DSV increases, the reproducing operation cannot be performed.

[0113] Fig. 24 shows an outline of a flow of a copying process. A reproducing apparatus denoted by reference numeral 41 reproduces data from an original disc. As described above, the disc 21 is a CD format disc. A special pattern is contained at a predetermined position in such a manner that merging bits selected in the EFM modulation when DSV is controlled according to the relation of an immediately preceded code symbol and a code symbol immediately followed thereby are different from merging bits selected in the EFM modulation when DSV is controlled according to that code symbol and a code symbol further immediately followed thereby. Reference numeral 43 represents an optical pickup. Reference numeral 44 represents a reproduction signal process portion. Reproduced data is supplied from the reproducing apparatus 41 to a recording process portion 52 of a recording apparatus 51. An optical pickup 53 records the reproduced data to a disc 54, for example a CD-R disc. The recorded contents of the original disc 21 are copied to the CD-R disc 54. The reproducing apparatus 41 and the recording apparatus 51 can use a recording and reproducing apparatus structured as a CD-R disc drive or a CD-RW disc drive.

[0114] As shown in Fig. 25, a sync detecting portion 46 of the reproducing process portion 44 detects a frame sync from a reproduced signal supplied from an input terminal 45. An EFM demodulator 47 EFM-demodulates the reproduced signal and supplies the EFM-demodulated reproduced data to a CIRC decoder 48. The CIRC decoder 48 corrects an error of the reproduced signal.

[0115] As described above, a special pattern shown in Fig. 2A, Fig. 2B, or Fig. 17A to Fig. 17E is contained at a predetermined position of the original disc 21 in such a manner that merging bits selected in the EFM modulation when DSV is controlled according to the relation of an immediately preceded code symbol and a code symbol immediately followed thereby are different from merging bits selected in the EFM modulation when DSV is controlled according to the relation of that code symbol and a code symbol further immediately followed thereby. The EFM modulator 12 of the mastering apparatus shown in Fig. 1 has the merging bit selecting portion 14 and the DSV controlling portion 15. As described above, the merging bit selecting portion 14 and the DSV controlling portion 15 perform the process for selecting merging bits according to not only the relation of an immediately preceded code symbol and a code symbol immediately followed thereby, but also the relation of that code symbol and a code symbol further immediately followed thereby that is pre-read. Thus, in such a special pattern, merging bits are added so that DSV finally converges to "0". Thus, the special pattern portion can be reproduced.

[0116] Fig. 26 shows an outline of the structure of a recording process portion 52. Data to be recorded is supplied from an input terminal 55 to a CIRC encoder 56. The CIRC encoder 56 performs a CIRC encoding process for the data to be recorded. Sub code data is

supplied from an input terminal 57 to a sub code encoder 58. The sub code encoder 58 formats the sub code. An output of the CIRC encoder 56 and an output of the sub code encoder 58 are supplied to a multiplexer 60. In addition, a frame sync is supplied from an input terminal 59 to the multiplexer 60. The multiplexer 60 arranges those data in a predetermined order. An output of the multiplexer 60 is supplied to an EFM modulator 61. The EFM modulator 61 performs an EFM modulating process for data that is output from the multiplexer 60.

[0117] As described above, the EFM modulator 61 normally selects merging bits of which DSV approaches to "0" according to the relation of an immediately preceded code symbol and a code symbol immediately followed thereby. Thus, when a reproduction signal of a portion of a special pattern at a predetermined position is sent to the EFM modulator 61, merging bits of which DSV approaches to "0" according to the relation of an immediately preceded code symbol and a code symbol immediately followed thereby are selected. As a result, DSV increases. The signal is recoded on a copy disc 54 such as a CD-R disc.

[0118] Thus, when the foregoing special pattern is recorded on the original disc 21, since a process for selecting merging bits according to not only the relation of an immediately preceded code symbol and a code symbol immediately followed thereby, but also the relation of that code symbol and a code symbol further immediately followed thereby is performed, in such a special pattern, merging bits are added so that DSV finally converges to "0". However, on the copied disc 54, merging bits of which DSV approaches to "0" according to the relation of an immediately preceded code symbol and a code symbol immediately followed thereby is selected. As a result, merging bits of which DSV increase are added. Thus, the reproducing operation cannot be performed.

[0119] In the foregoing example, on the original disc 21, the process for selecting merging bits according to not only the relation of an immediately preceded code symbol and a code symbol immediately followed thereby, but also the relation of that code symbol and a code symbol further immediately followed thereby that is preread is performed. However, if the special pattern has been predetermined, merging bits may be added so that merging bits added to the special pattern are different from merging bits added to the other portion. In this case, as the EFM modulator 12, a conventional modulator that selects merging bits of which DSV approaches to "0" according to the relation of an immediately preceded code symbol and a code symbol immediately followed thereby can be used.

[0120] The permission and prohibition of the use of contents other than the special pattern portion can be controlled. In other words, from a disc produced by the master apparatus according to the present invention, the data pattern portion can be reproduced. On the other hand, when a disc is produced by a conventional encoder using an original disc that has been produced by the master apparatus, the special pattern portion cannot be reproduced. Thus, depending on whether or not the pattern portion can be read, the disc is detected as an original disc or a copy thereof. According to the detected result, it is determined whether or not contents recorded in other than the data pattern portion can be used. As a result, contents of a copied disc can be prohibited from being used.

[0121] The special pattern would be placed in a key data portion of encrypted contents. From a copied disc, the key data portion would be prohibited from being reproduced.

[0122] Although the present invention has been shown and described with respect to a best mode embodiment thereof, it should be understood by those skilled in the art that the foregoing and various other changes, omissions, and additions in the form and detail thereof may be made therein without departing from the spirit and scope of the present invention. For example, as a modulating system other than EFM, the present invention can be applied to EFM Plus. The EFM Plus is a system that converts a data symbol of eight bits into a code symbol of 16 bits without need to use merging bits. In the EFM Plus, there are special data patterns of which DSV increases. Thus, when an encoder that has a modified code conversion table modified from the standard code conversion table is used, even if a special data pattern is used, DSV can be prevented from increasing. Thus, it can be determined whether or not a disc to be used is an original disc of which data was recorded using an encoder according to the present invention or a copied disc of which data was recorded using a conventional encoder.

[0123] The present invention can be also applied to a multi-session optical disc on which for example CD-DA formatted data and CD-ROM formatted data are recorded. As information that is recorded to an optical disc, there are various types of data such as audio data, video data, still picture data, character data, computer graphic data, game software, and computer programs. Thus, the present invention can be applied to for example a DVD video disc and a DVD-ROM disc. In addition, the present invention can be applied to not only a disc-shaped data recording medium, but also a card-shaped data recording medium.

[0124] In the foregoing example, an original disc is produced by the mastering apparatus. Alternatively, an original disc may be produced with a CD-R disc or a CD-RW disc. When a special pattern is recorded, since it does not require to physically deform a disc with for example pits, even if an original disc is a recording medium using wobble pits such as a CD-R disc or a CD-RW disc, a copy can be protected.

[0125] As is clear from the foregoing description, according to the present invention, a special pattern is recorded on a recording medium in such a manner that merging bits selected in the EFM modulation when DSV

is controlled according to the relation of an immediately preceded code symbol and a code symbol immediately followed thereby are different from merging bits selected in the EFM modulation when DSV is controlled according to the relation of those code symbol and a code symbol further immediately followed thereby. The EFM modulating portion of the master apparatus that produces an original CD selects merging bits according to not only the relation of an immediately preceded code symbol and a code symbol immediately followed thereby, but also the relation of that code symbol and a code symbol further immediately followed thereby that is pre-read. Thus, even if an original recording medium produced by the master apparatus contains such a special pattern, merging bits are selected so that DSV converges to "0". In contrast, when a CD-R recording apparatus or the like copies a data of a disc, the EFM modulating portion of the CD-R recording apparatus selects merging bits of which DSV approaches "0" according to only the relation of an immediately preceded code symbol and a code symbol immediately followed thereby, not the relation of that code symbol and a code symbol further immediately followed thereby. Thus, in the special pattern, since DSV increases, the reproducing operation cannot be performed. As a result, the copying operation can be restricted.

[0126] According to the present invention, without need to physically deform a disc with for example pits, a copying operation can be prohibited for not only a disc having wobble pits, but also an original recording medium that is a CR-R or CD-RW.

[0127] In addition, according to the present invention, since data cannot be reproduced from a copied recording medium, data of an original recording medium can be prevented from being directly copied.

[0128] In addition, according to the present invention, since a defect is not intentionally placed on an original medium, the present invention can be used as a format standard.

Claims

1. A recording method for converting m-bit data into an n-bit (where n > m) data symbol whose run length is restricted and placing a connection bit after the m-bit data symbol so that the cumulative value of DC components per unit time becomes small, the recording method comprising the steps of:

   selecting a first connection bit to be added to an immediately preceded data symbol from a plurality of connection bits according to at least one first connection bit that can be added between the immediately preceded data symbol and a first data symbol immediately followed thereby and according to at least one second connection bit that can be added between the first data symbol and at least one second data symbol immediately followed thereby;
   adding the selected first connection bit to the immediately preceded data symbol so as to generate record data; and
   recording the generated record data on a recording medium.

2. The recording method as set forth in claim 1,
   wherein the selecting step comprises the steps of:

   selecting at least one first connection bit that can be added between the immediately preceded data symbol and the first data symbol immediately followed thereby;
   selecting at least one second connection bit that can be added between the first data symbol and at least one second data symbol immediately followed thereby; and
   selecting the first connection bit from the selected first connection bit and the selected second connection bit so that the cumulative value of the DC components becomes small.

3. The recording method as set forth in claim 2,
   wherein the first connection bit selecting step is performed by selecting the first connection bit so that. when the selected first connection bit and the selected second connection bit are combined, the cumulative value of the DC components becomes small.

4. A recording method for converting m-bit data into an n-bit (where n > m) data symbol whose run length is restricted and adding a connection bit after the m-bit data symbol so that the cumulative value of DC components per unit time becomes small, the recording method comprising the steps of:

   when an immediately preceded data symbol is a special data symbol, selecting a first connection bit to be added to the immediately preceded data symbol from a plurality of connection bits according to at least one first connection bit that can be added between the immediately preceded data symbol and a first data symbol immediately followed thereby and according to at least one second connection bit that can be added between the first data symbol and at least one second data symbol immediately followed thereby;
   adding the selected first connection bit to the immediately preceded data symbol so as to generate record data; and
   recording the generated record data on a recording medium.

5. The recording method as set forth in claim 4, wherein the selecting step comprises the steps of:

selecting at least one first connection bit that can be added between the immediately preceded data symbol and the first data symbol immediately followed thereby;
selecting at least one second connection bit that can be added between the first data symbol and at least one second data symbol immediately followed thereby; and
selecting the first connection bit from the selected first connection bit and the selected second connection bit so that the cumulative value of the DC components becomes small.

6. The recording method as set forth in claim 5, wherein the first connection bit selecting step is performed by selecting the first connection bit so that when the selected first connection bit and the selected second connection bit are combined, the cumulative value of the DC components becomes small.

7. The recording method as set forth in claim 4, wherein when the first data symbol is selected according to the immediately preceded data symbol and the first data symbol, with the special data symbol, the second connection bit added between the first data symbol and the second data symbol is unconditionally selected.

8. The recording method as set forth in claim 4, wherein the m-bit data is modulated according to the 8-14 modulating system.

9. A recording method for converting m-bit data into n-bit (where n > m) data whose run length is restricted and recording the converted data on a recording medium, the recording method comprising the step of:

selecting first n-bit data according to an immediately preceded n-bit data, first n-bit data immediately followed thereby, and second n-bit data immediately followed thereby so that the cumulative value of DC components per unit time becomes small.

10. The recording method as set forth in claim 9, wherein the n-bit data is composed of an n1-bit data symbol and n2-bit (= n - n1) connection bits immediately followed thereby and selected from a plurality of connection bits so that the cumulative value of DC components per unit time becomes small, and
wherein the recording method further comprises the step of:

selecting a first connection bit to be added to the immediately preceded data symbol according to at least one connection bit that can be added between the immediately preceded data symbol and the first data symbol and at least one second connection bit that can be added between the first data symbol and the second data symbol.

11. The recording method as set forth in claim 10, wherein the selecting step comprises the steps of:

selecting at least one first connection bit that can be added between the immediately preceded data symbol and the first data symbol immediately followed thereby;
selecting at least one second connection bit that can be added between the first data symbol and the second data symbol; and
selecting the first connection bit from the selected first connection bit and the second connection bit so that the cumulative value of the DC components becomes small.

12. The recording method as set forth in claim 11, wherein the first connection bit selecting step is performed by selecting the first connection bit so that when the selected first connection bit and the selected second connection bit are combined, the cumulative value of the DC components becomes small.

13. The recording method as set forth in claim 9, wherein the m-bit data is modulated according to the 8-14 modulating system.

14. The recording method as set forth in claim 9, wherein the m-bit data is modulated according to the 8-16 modulating system.

15. The recording method as set forth in claim 9, wherein the n-bit data is composed of an n1-bit data symbol and n2-bit (= n - n1) connection bits immediately followed thereby and selected from a plurality of connection bits so that the cumulative value of DC components per unit time becomes small, and
wherein the recording method further comprises the step of:

when the immediately preceded data symbol is a special data symbol, selecting a first connection bit to be added to the immediately preceded data symbol according to at least one connection bit that can be added between the im-

mediately preceded data symbol and the first data symbol and at least one second connection bit that can be added between the first data symbol and the second data symbol.

16. The recording method as set forth in claim 15, wherein the selecting step comprises the steps of:

selecting at least one first connection bit that can be added between the immediately preceded data symbol and the first data symbol immediately followed thereby;
selecting at least one second connection bit that can be added between the first data symbol and the second data symbol; and
selecting the first connection bit from the selected first connection bit and the second connection bit so that the cumulative value of the DC components becomes small.

17. The recording method as set forth in claim 16, wherein the first connection bit selecting step is performed by selecting the first connection bit so that when the selected first connection bit and the selected second connection bit are combined, the cumulative value of the DC components becomes small.

18. The recording method as set forth in claim 15, wherein when the first data symbol is selected according to the immediately preceded data symbol and the first data symbol, with the special data symbol, the second connection bit added between the first data symbol and the second data symbol is unconditionally selected.

19. A recording apparatus, comprising:

an encoding process portion for performing an encoding process for input data;
a converting portion for converting m-bit data that is output from the encoding processing portion into n-bit (where n > m) data whose run length is restricted by selecting first n-bit data according to an immediately preceded n-bit data, first n-bit data immediately followed thereby, and second n-bit data immediately followed thereby so that the cumulative value of DC components per unit time becomes small; and
a recording portion for recording data that is output from the converting portion on a recording medium.

20. The recording apparatus as set forth in claim 19, wherein the n-bit data is composed of an n1-bit data symbol and n2-bit (= n - n1) connection bits immediately followed thereby and selected from a plurality of connection bits so that the cumulative value of DC components per unit time becomes small, and

wherein the converting portion is configured to select a first connection bit to be added to the immediately preceded data symbol according to at least one connection bit that can be added between the immediately preceded data symbol and the first data symbol and at least one second connection bit that can be added between the first data symbol and the second data symbol.

21. The recording apparatus as set forth in claim 20, wherein the converting portion is configured to select at least one first connection bit that can be added between the immediately preceded data symbol and the first data symbol immediately followed thereby, select at least one second connection bit that can be added between the first data symbol and the second data symbol, and select the first connection bit from the selected first connection bit and the second connection bit so that the cumulative value of the DC components becomes small.

22. The recording apparatus as set forth in claim 21, wherein the converting portion is configured to select the first connection bit so that when the selected first connection bit and the selected second connection bit are combined, the cumulative value of the DC components becomes small.

23. The recording apparatus as set forth in claim 19, wherein the m-bit data is modulated according to the 8-14 modulating system.

24. The recording apparatus as set forth in claim 19, wherein the m-bit data is modulated according to the 8-16 modulating system.

25. The recording apparatus as set forth in claim 19. wherein the n-bit data is composed of an n1-bit data symbol and n2-bit (= n - n1) connection bits immediately followed thereby and selected from a plurality of connection bits so that the cumulative value of DC components per unit time becomes small, and

wherein the converting portion is configured to select a first connection bit to be added to the immediately preceded data symbol according to at least one connection bit that can be added between the immediately preceded data symbol and the first data symbol and at least one second connection bit that can be added between the first data symbol and the second data symbol when the immediately preceded data symbol is a special data symbol.

26. The recording apparatus as set forth in claim 25, wherein the converting portion is configured

to select at least one first connection bit that can be added between the immediately preceded data symbol and the first data symbol immediately followed thereby, select at least one second connection bit that can be added between the first data symbol and the second data symbol, and select the first connection bit from the selected first connection bit and the second connection bit so that the cumulative value of the DC components becomes small.

27. The recording apparatus as set forth in claim 26,
wherein the converting portion is configured to select the first connection bit so that when the selected first connection bit and the selected second connection bit are combined, the cumulative value of the DC components becomes small.

28. The recording apparatus as set forth in claim 25,
wherein when the first data symbol is selected according to the immediately preceded data symbol and the first data symbol, with the special data symbol, the second connection bit added between the first data symbol and the second data symbol is unconditionally selected.

29. A recording medium on which when m-bit data is converted into n-bit (where n > m) data whose run length is restricted, first n-bit data is selected according to an immediately preceded n-bit data, first n-bit data immediately followed thereby, and second n-bit data immediately followed thereby so that the cumulative value of DC components per unit time becomes small and the selected first n-bit data is recorded after the immediately preceded n-bit data.

30. The recording medium as set forth in claim 29,
wherein the n-bit data is composed of an n1-bit data symbol and n2-bit (= n - n1) connection bits immediately followed thereby and selected from a plurality of connection bits so that the cumulative value of DC components per unit time becomes small, and
wherein a first connection bit to be added to the immediately preceded data symbol is selected according to at least one connection bit that can be added between the immediately preceded data symbol and the first data symbol and at least one second connection bit that can be added between the first data symbol and the second data symbol and recorded on the recording medium.

31. The recording medium as set forth in claim 30,
wherein at least one first connection bit that can be added between the immediately preceded data symbol and the first data symbol immediately followed thereby is selected,
wherein at least one second connection bit that can be added between the first data symbol and the second data symbol is selected,
wherein the first connection bit is selected from the selected first connection bit and the second connection bit so that the cumulative value of the DC components becomes small, and
wherein the resultantly selected first connection bit is recorded on the recording medium.

32. The recording medium as set forth in claim 31,
wherein the first connection bit is selected so that when the selected first connection bit and the selected second connection bit are combined, the cumulative value of the DC components becomes small, and
wherein the resultantly selected first connection bit is recorded on the recording medium.

33. The recording medium as set forth in claim 29,
wherein the m-bit data is modulated according to the 8-14 modulating system and recorded on the recording medium.

34. The recording medium as set forth in claim 29,
wherein the m-bit data is modulated according to the 8-16 modulating system and recorded on the recording medium.

35. The recording medium as set forth in claim 29,
wherein the n-bit data is composed of an n1-bit data symbol and n2-bit (= n - n1) connection bits immediately followed thereby and selected from a plurality of connection bits so that the cumulative value of DC components per unit time becomes small, and
wherein when the immediately preceded data symbol is a special data symbol, a first connection bit to be added to the immediately preceded data symbol is selected according to at least one connection bit that can be added between the immediately preceded data symbol and the first data symbol and at least one second connection bit that can be added between the first data symbol and the second data symbol and recorded on the recording medium.

36. The recording medium as set forth in claim 35,
wherein at least one first connection bit that can be added between the immediately preceded data symbol and the first data symbol immediately followed thereby is selected,
wherein at least one second connection bit that can be added between the first data symbol and the second data symbol is selected, and
wherein the first connection bit is selected from the selected first connection bit and the second connection bit so that the cumulative value of the DC components becomes small, and

wherein the resultantly selected first connection bit is recorded on the recording medium.

37. The recording medium as set forth in claim 36,
wherein the first connection bit is selected so that when the selected first connection bit and the selected second connection bit are combined, the cumulative value of the DC components becomes small, and
wherein the resultantly selected first connection bit is recorded on the record medium.

38. The recording medium as set forth in claim 35,
wherein when the first data symbol is selected according to the immediately preceded data symbol and the first data symbol, with the special data symbol, the second connection bit added between the first data symbol and the second data symbol is unconditionally selected.

39. A data converting method, comprising the step of:
when m-bit data is converted into n-bit (where n > m) data whose run length is restricted, selecting first n-bit data according to an immediately preceded n-bit data, first n-bit data immediately followed thereby, and second n-bit data immediately followed thereby so that the cumulative value of DC components per unit time becomes small.

40. The data converting method as set forth in claim 39,
wherein the n-bit data is composed of an n1-bit data symbol and n2-bit (= n - n1) connection bits immediately followed thereby and selected from a plurality of connection bits so that the cumulative value of DC components per unit time becomes small, and
wherein the data converting method further comprises the step of:

selecting a first connection bit to be added to the immediately preceded data symbol according to at least one connection bit that can be added between the immediately preceded data symbol and the first data symbol and at least one second connection bit that can be added between the first data symbol and the second data symbol.

41. The data converting method as set forth in claim 40,
wherein the selecting step comprises the steps of:

selecting at least one first connection bit that can be added between the immediately preceded data symbol and the first data symbol immediately followed thereby;
selecting at least one second connection bit that can be added between the first data symbol and the second data symbol; and
selecting the first connection bit from the selected first connection bit and the second connection bit so that the cumulative value of the DC components becomes small.

42. The data converting method as set forth in claim 41,
wherein the first connection bit selecting step is performed by selecting the first connection bit so that when the selected first connection bit and the selected second connection bit are combined, the cumulative value of the DC components becomes small.

43. The data converting method as set forth in claim 39,
wherein the m-bit data is modulated according to the 8-14 modulating system.

44. The data converting method as set forth in claim 39,
wherein the m-bit data is modulated according to the 8-16 modulating system.

45. The data converting method as set forth in claim 39,
wherein the n-bit data is composed of an n1-bit data symbol and n2-bit (= n - n1) connection bits immediately followed thereby and selected from a plurality of connection bits so that the cumulative value of DC components per unit time becomes small, and
wherein the data converting method further comprises the step of:

when the immediately preceded data symbol is a special data symbol, selecting a first connection bit to be added to the immediately preceded data symbol according to at least one connection bit that can be added between the immediately preceded data symbol and the first data symbol and at least one second connection bit that can be added between the first data symbol and the second data symbol.

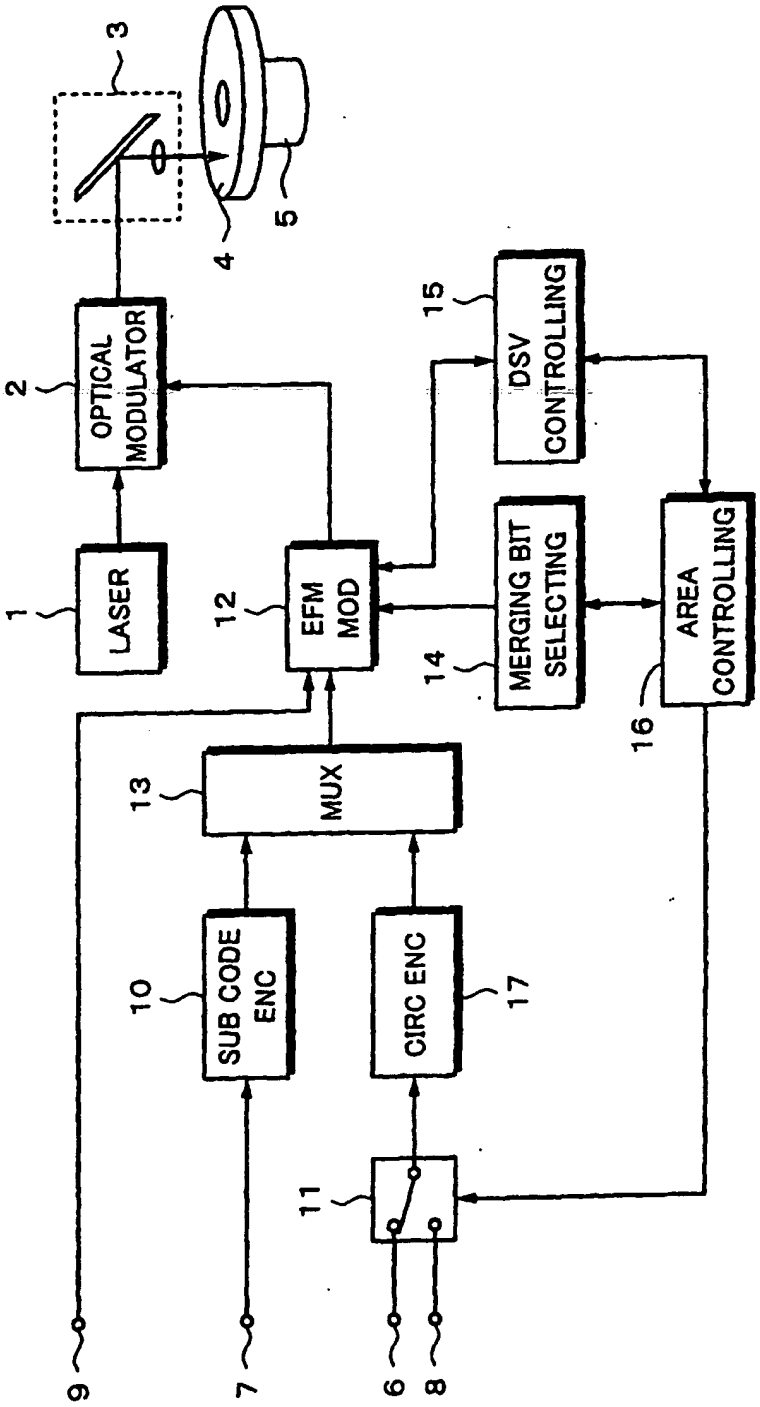
46. The data converting method as set forth in claim 45,
wherein the selecting step comprises the steps of:

selecting at least one first connection bit that can be added between the immediately preceded data symbol and the first data symbol immediately followed thereby;
selecting at least one second connection bit that can be added between the first data symbol and the second data symbol; and
selecting the first connection bit from the selected first connection bit and the second connection bit so that the cumulative value of the DC components becomes small.

47. The data converting method as set forth in claim 46, wherein the first connection bit selecting step is performed by selecting the first connection bit so that when the selected first connection bit and the selected second connection bit are combined, the cumulative value of the DC components becomes small.

48. The data converting method as set forth in claim 35, wherein when the first data symbol is selected according to the immediately preceded data symbol and the first data symbol, with the special data symbol, the second connection bit added between the first data symbol and the second data symbol is unconditionally selected.

Fig. 1


3
4
5
2
OPTICAL MODULATOR
15
DSV CONTROLLING
1
LASER
12
EFM MOD
14
MERGING BIT SELECTING
16
AREA CONTROLLING
13
MUX
10
SUB CODE ENC
17
CIRC ENC
11
9
7
6
8

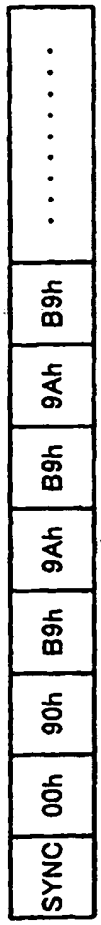

SYNC
00h
90h
B9h
9Ah
B9h
9Ah
B9h
. . . . . .

Fig. 2A

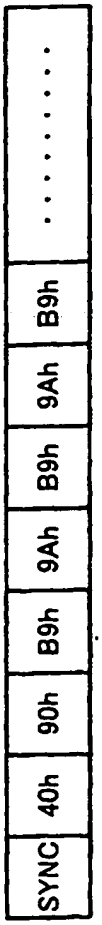

SYNC
40h
90h
B9h
9Ah
B9h
9Ah
B9h
. . . . . .

Fig. 2B

Fig. 3

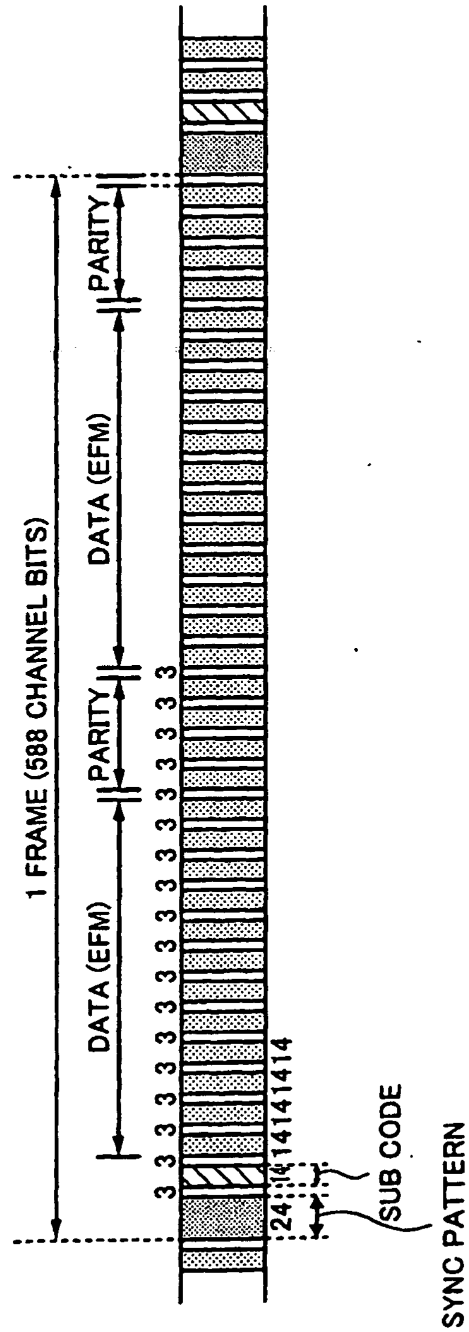

1 FRAME (588 CHANNEL BITS)
DATA (EFM)
PARITY
DATA (EFM)
PARITY
SUB CODE
SYNC PATTERN
24
14
3

Fig. 4

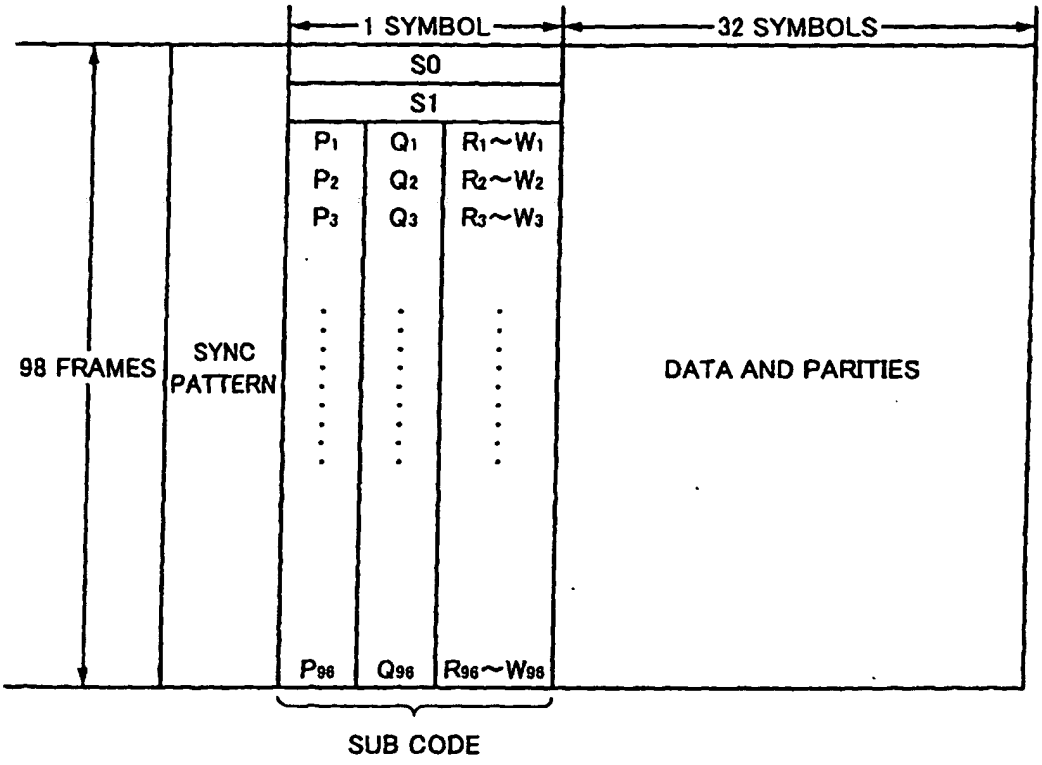
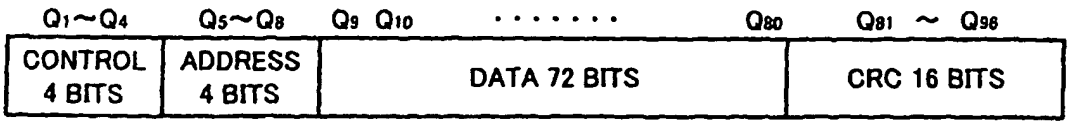

1 SYMBOL
32 SYMBOLS
S0
S1
P1 Q1 R1~W1
P2 Q2 R2~W2
P3 Q3 R3~W3
98 FRAMES
SYNC PATTERN
DATA AND PARITIES
P98 Q98 R96~W98
SUB CODE

Fig. 5


Q1~Q4
Q5~Q8
Q9 Q10
Q80
Q81 ~ Q96
CONTROL 4 BITS
ADDRESS 4 BITS
DATA 72 BITS
CRC 16 BITS

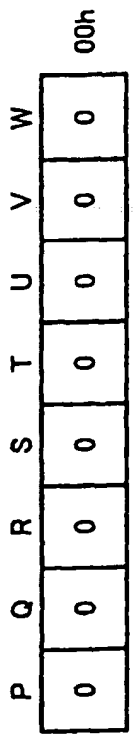


Fig. 6A

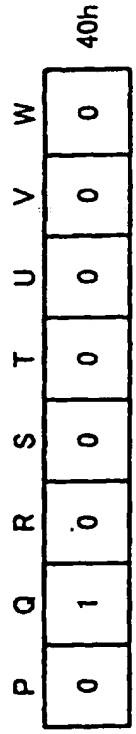


Fig. 6B

Fig. 7

HEXADECIMAL	DECIMAL	DATA SYMBOL d1.....d8	CODE SYMBOL C1.....C14
00h	000	00000000	01001000100000
01h	001	00000001	10000100000000
02h	002	00000010	10010000100000
03h	003	00000011	10001000100000
04h	004	00000100	01000100000000
05h	005	00000101	00000100010000
06h	006	00000110	00010000100000
07h	007	00000111	00100100000000
08h	008	00001000	01001001000000
09h	009	00001001	10000001000000
0Ah	010	00001010	10010001000000
0Bh	011	00001011	10001001000000
0Ch	012	00001100	01000001000000
0Dh	013	00001101	00000001000000
0Eh	014	00001110	00010001000000
0Fh	015	00001111	00100001000000
10h	016	00010000	10000000100000
11h	017	00010001	10000010000000
12h	018	00010010	10010010000000
13h	019	00010011	00100000100000
14h	020	00010100	01000010000000
15h	021	00010101	00000010000000
16h	022	00010110	00010010000000
17h	023	00010111	00100010000000
18h	024	00011000	01001000010000
19h	025	00011001	10000000010000
1Ah	026	00011010	10010000010000
1Bh	027	00011011	10001000010000
1Ch	028	00011100	01000000010000
1Dh	029	00011101	00001000010000
1Eh	030	00011110	00010000010000
1Fh	031	00011111	00100000010000
20h	032	00100000	00000000100000
21h	033	00100001	10000100001000
22h	034	00100010	00001000100000
23h	035	00100011	00100100100000
24h	036	00100100	01000100001000
25h	037	00100101	00000100001000
26h	038	00100110	01000000100000
27h	039	00100111	00100100001000
28h	040	00101000	01001001001000
29h	041	00101001	10000001001000
2Ah	042	00101010	10010001001000
2Bh	043	00101011	10001001001000
2Ch	044	00101100	01000001001000
2Dh	045	00101101	00000001001000
2Eh	046	00101110	00010001001000
2Fh	047	00101111	00100001001000

Fig. 8

30h	048	00110000	000001000000000
31h	049	00110001	10000010001000
32h	050	00110010	10010010001000
33h	051	00110011	10000100010000
34h	052	00110100	01000010001000
35h	053	00110101	00000010001000
36h	054	00110110	00010010001000
37h	055	00110111	00100010001000
38h	056	00111000	01001000001000
39h	057	00111001	10000000001000
3Ah	058	00111010	10010000001000
3Bh	059	00111011	10001000001000
3Ch	060	00111100	01000000001000
3Dh	061	00111101	00001000001000
3Eh	062	00111110	00010000001000
3Fh	063	00111111	00100000001000
40h	064	01000000	01001000100100
41h	065	01000001	10000100100100
42h	066	01000010	10010000100100
43h	067	01000011	10001000100100
44h	068	01000100	01000100100100
45h	069	01000101	00000000100100
46h	070	01000110	00010000100100
47h	071	01000111	00100100100100
48h	072	01001000	01001001000100
49h	073	01001001	10000001000100
4Ah	074	01001010	10010001000100
4Bh	075	01001011	10001001000100
4Ch	076	01001100	01000001000100
4Dh	077	01001101	00000001000100
4Eh	078	01001110	00010001000100
4Fh	079	01001111	00100001000100
50h	080	01010000	10000000100100
51h	081	01010001	10000010000100
52h	082	01010010	10010010000100
53h	083	01010011	00100000100100
54h	084	01010100	01000010000100
55h	085	01010101	00000010000100
56h	086	01010110	00010010000100
57h	087	01010111	00100010000100
58h	088	01011000	01001000000100
59h	089	01011001	10000000000100
5Ah	090	01011010	10010000000100
5Bh	091	01011011	10001000000100
5Ch	092	01011100	01000000000100
5Dh	093	01011101	00001000000100
5Eh	094	01011110	00010000000100
5Fh	095	01011111	00100000000100
60h	096	01100000	01001000100010
61h	097	01100001	10000100100010

Fig. 9

62h	098	01100010	10010000100010
63h	099	01100011	10001000100010
64h	100	01100100	01000100100010
65h	101	01100101	00000000100010
66h	102	01100110	01000000100100
67h	103	01100111	00100100100010
68h	104	01101000	01001001000010
69h	105	01101001	10000001000010
6Ah	106	01101010	10010001000010
6Bh	107	01101011	10001001000010
6Ch	108	01101100	01000001000010
6Dh	109	01101101	00000001000010
6Eh	110	01101110	00010001000010
6Fh	111	01101111	00100001000010
70h	112	01110000	10000000100010
71h	113	01110001	10000010000010
72h	114	01110010	10010010000010
73h	115	01110011	00100000100010
74h	116	01110100	01000010000010
75h	117	01110101	00000010000010
76h	118	01110110	00010010000010
77h	119	01110111	00100010000010
78h	120	01111000	01001000000010
79h	121	01111001	00001001001000
7Ah	122	01111010	10010000000010
7Bh	123	01111011	10001000000010
7Ch	124	01111100	01000000000010
7Dh	125	01111101	00001000000010
7Eh	126	01111110	00010000000010
7Fh	127	01111111	00100000000010
80h	128	10000000	01001000100001
81h	129	10000001	10000100100001
82h	130	10000010	10010000100001
83h	131	10000011	10001000100001
84h	132	10000100	01000100100001
85h	133	10000101	00000000100001
86h	134	10000110	00010000100001
87h	135	10000111	00100100100001
88h	136	10001000	01001001000001
89h	137	10001001	10000001000001
8Ah	138	10001010	10010001000001
8Bh	139	10001011	10001001000001
8Ch	140	10001100	01000001000001
8Dh	141	10001101	00000001000001
8Eh	142	10001110	00010001000001
8Fh	143	10001111	00100001000001
90h	144	10010000	10000000100001
91h	145	10010001	10000010000001
92h	146	10010010	10010010000001
93h	147	10010011	00100000100001

Fig. 10

94h	148	10010100	01000010000001
95h	149	10010101	00000010000001
96h	150	10010110	00010010000001
97h	151	10010111	00100010000001
98h	152	10011000	01001000000001
99h	153	10011001	10000010010000
9Ah	154	10011010	10010000000001
9Bh	155	10011011	10001000000001
9Ch	156	10011100	01000010010000
9Dh	157	10011101	00001000000001
9Eh	158	10011110	00010000000001
9Fh	159	10011111	00100010010000
A0h	160	10100000	00001000100001
A1h	161	10100001	10000100001001
A2h	162	10100010	01000100010000
A3h	163	10100011	00000100100001
A4h	164	10100100	01000100001001
A5h	165	10100101	00000100001001
A6h	166	10100110	01000000100001
A7h	167	10100111	00100100001001
A8h	168	10101000	01001001001001
A9h	169	10101001	10000001001001
AAh	170	10101010	10010001001001
ABh	171	10101011	10001001001001
ACh	172	10101100	01000001001001
ADh	173	10101101	00000001001001
AEh	174	10101110	00010001001001
AFh	175	10101111	00100001001001
B0h	176	10110000	00000100100000
B1h	177	10110001	10000010001001
B2h	178	10110010	10010010001001
B3h	179	10110011	00100100010000
B4h	180	10110100	01000010001001
B5h	181	10110101	00000010001001
B6h	182	10110110	00010010001001
B7h	183	10110111	00100010001001
B8h	184	10111000	01001000001001
B9h	185	10111001	10000000001001
BAh	186	10111010	10010000001001
BBh	187	10111011	10001000001001
BCh	188	10111100	01000000001001
BDh	189	10111101	00001000001001
BEh	190	10111110	00010000001001
BFh	191	10111111	00100000001001
C0h	192	11000000	01000100100000
C1h	193	11000001	10000100010001
C2h	194	11000010	10010010010000
C3h	195	11000011	00001000100100
C4h	196	11000100	01000100010001
C5h	197	11000101	00000100010001

Fig. 11

C6h	198	11000110	000010010010000
C7h	199	11000111	00100100010001
C8h	200	11001000	00001001000001
C9h	201	11001001	10000100000001
CAh	202	11001010	00001001000100
CBh	203	11001011	00001001000000
CCh	204	11001100	01000100000001
CDh	205	11001101	00000100000001
CEh	206	11001110	00000010010000
CFh	207	11001111	00100100000001
D0h	208	11010000	00000100100100
D1h	209	11010001	10000010010001
D2h	210	11010010	10010010010001
D3h	211	11010011	10000100100000
D4h	212	11010100	01000010010001
D5h	213	11010101	00000010010001
D6h	214	11010110	00010010010001
D7h	215	11010111	00100010010001
D8h	216	11011000	01001000010001
D9h	217	11011001	10000000010001
DAh	218	11011010	10010000010001
DBh	219	11011011	10001000010001
DCh	220	11011100	01000000010001
DDh	221	11011101	00001000010001
DEh	222	11011110	00010000010001
DFh	223	11011111	00100000010001
E0h	224	11100000	01000100000010
E1h	225	11100001	00000100000010
E2h	226	11100010	10000100010010
E3h	227	11100011	00100100000010
E4h	228	11100100	01000100010010
E5h	229	11100101	00000100010010
E6h	230	11100110	01000000100010
E7h	231	11100111	00100100010010
E8h	232	11101000	10000100000010
E9h	233	11101001	10000100000100
EAh	234	11101010	00001001001001
EBh	235	11101011	00001001000010
ECh	236	11101100	01000100000100
EDh	237	11101101	00000100000100
EEh	238	11101110	00010000100010
EFh	239	11101111	00100100000100
F0h	240	11110000	00000100100010
F1h	241	11110001	10000010010010
F2h	242	11110010	10010010010010
F3h	243	11110011	00001000100010
F4h	244	11110100	01000010010010
F5h	245	11110101	00000010010010
F6h	246	11110110	00010010010010
F7h	247	11110111	00100010010010

Fig. 12

F8h	248	11111000	01001000010010
F9h	249	11111001	10000000010010
FAh	250	11111010	10010000010010
FBh	251	11111011	10001000010010
FCh	252	11111100	01000000010010
FDh	253	11111101	00001000010010
FEh	254	11111110	00010000010010
FFh	255	11111111	00100000010010

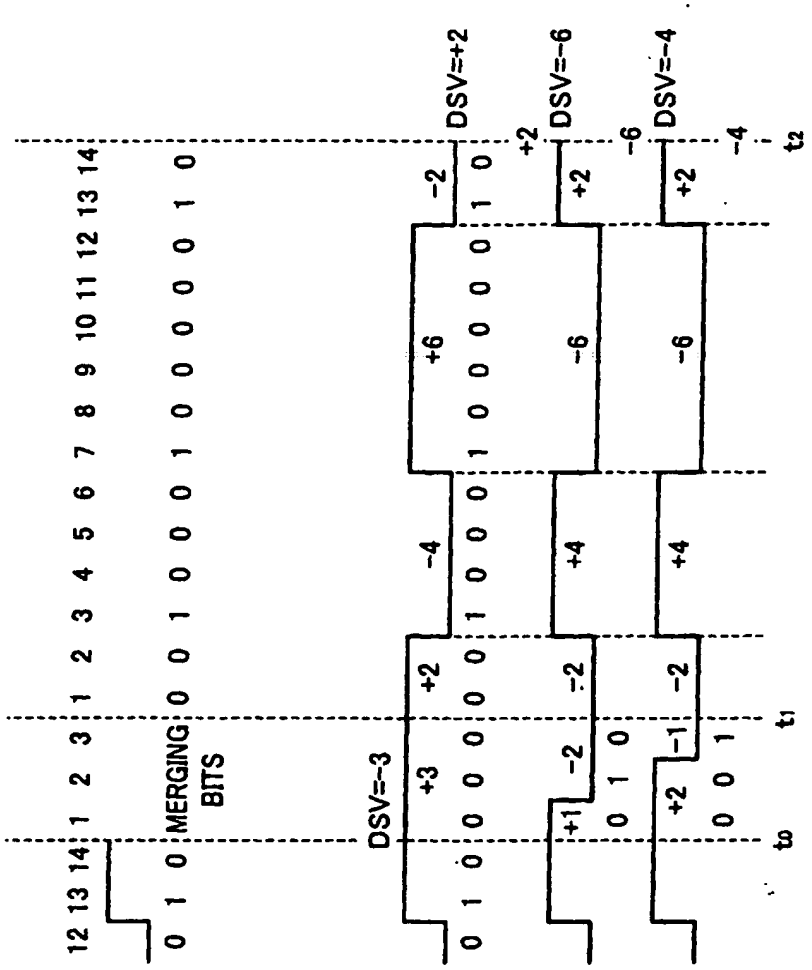


Fig. 13A

Fig. 13B

Fig. 13C

Fig. 13D

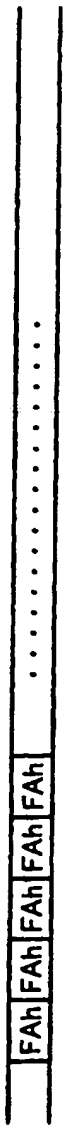


Fig. 14A

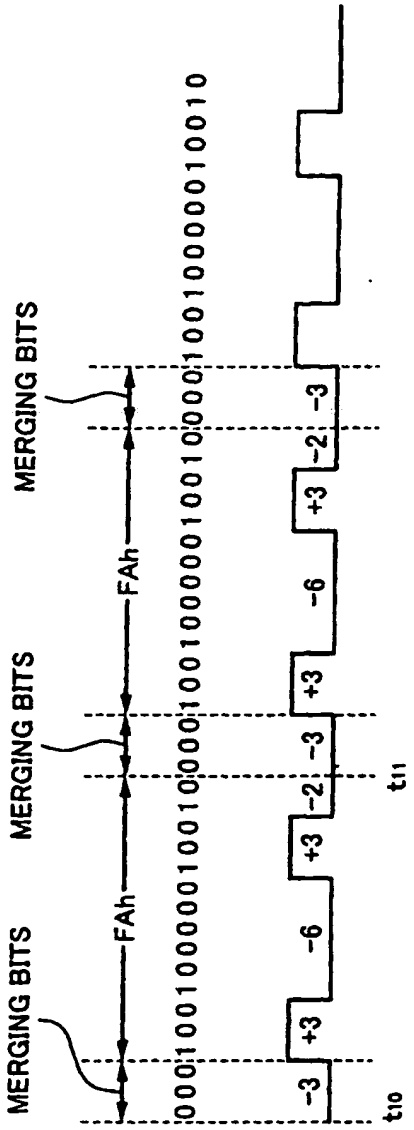


Fig. 14B

Fig. 14C

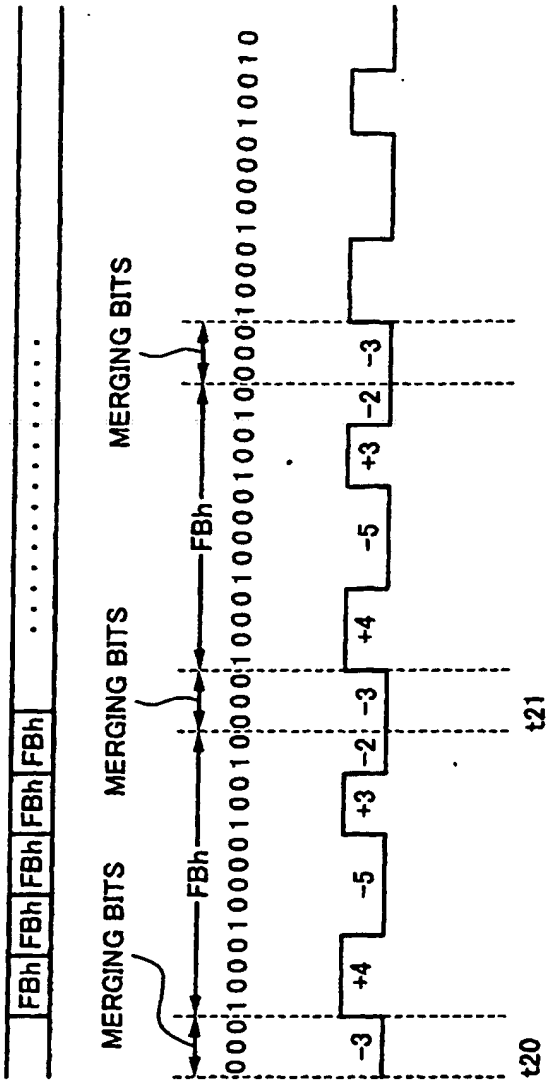


Fig. 15A

Fig. 15B

Fig. 15C

Fig. 16A

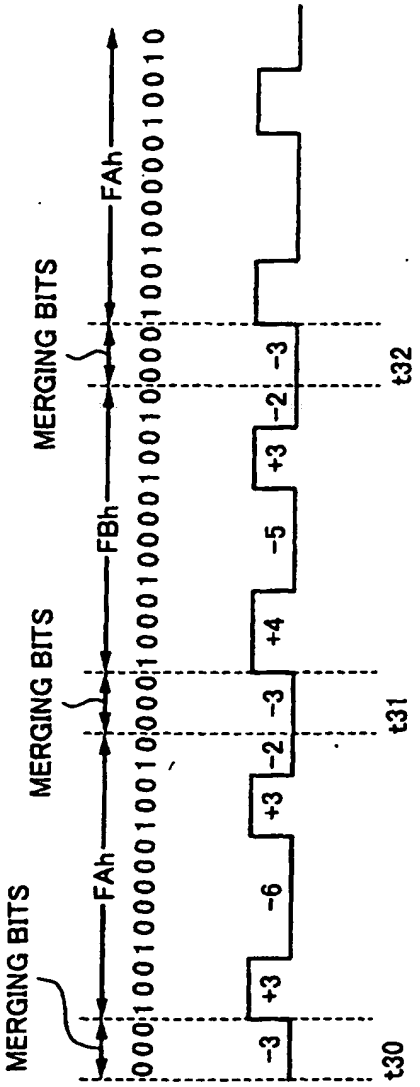


Fig. 16B

Fig. 16C

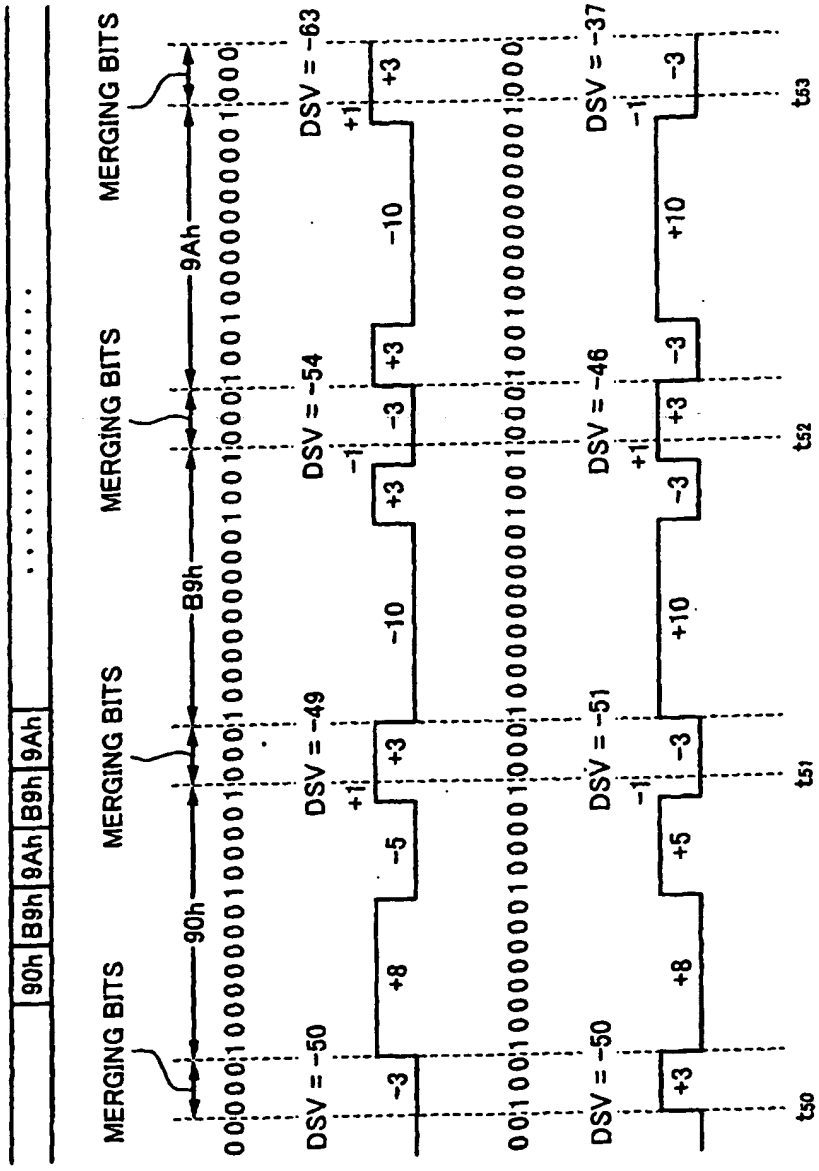


Fig. 17A

Fig. 17B

Fig. 17C

Fig. 17D

Fig. 17E

Fig. 18

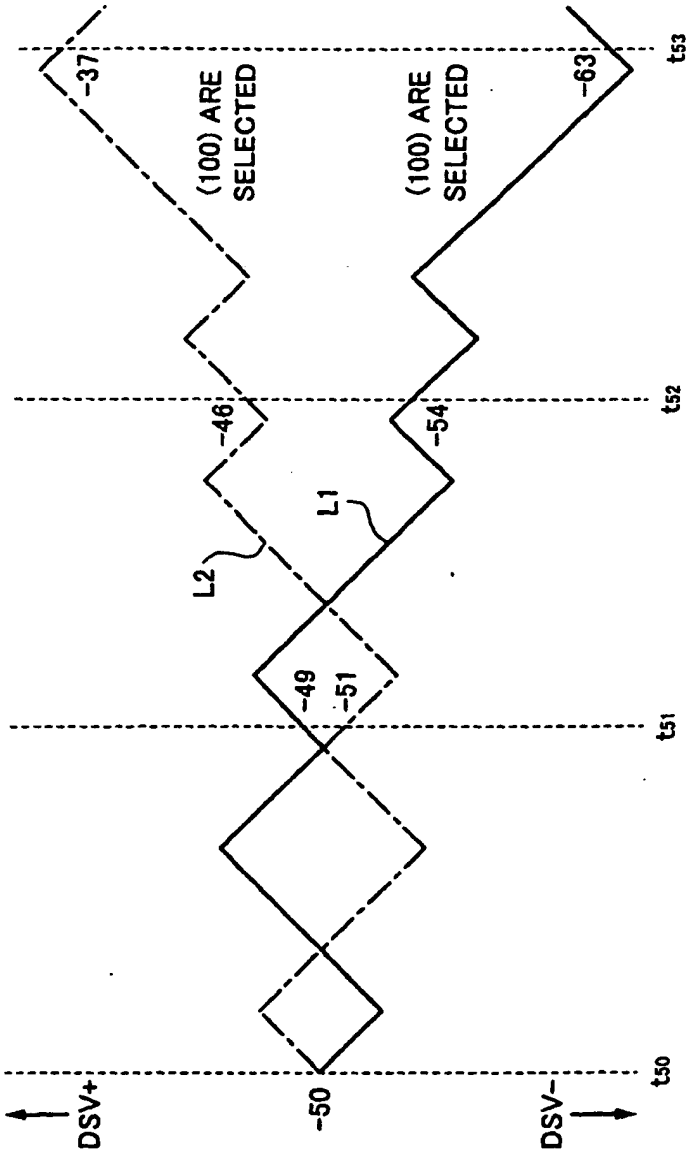
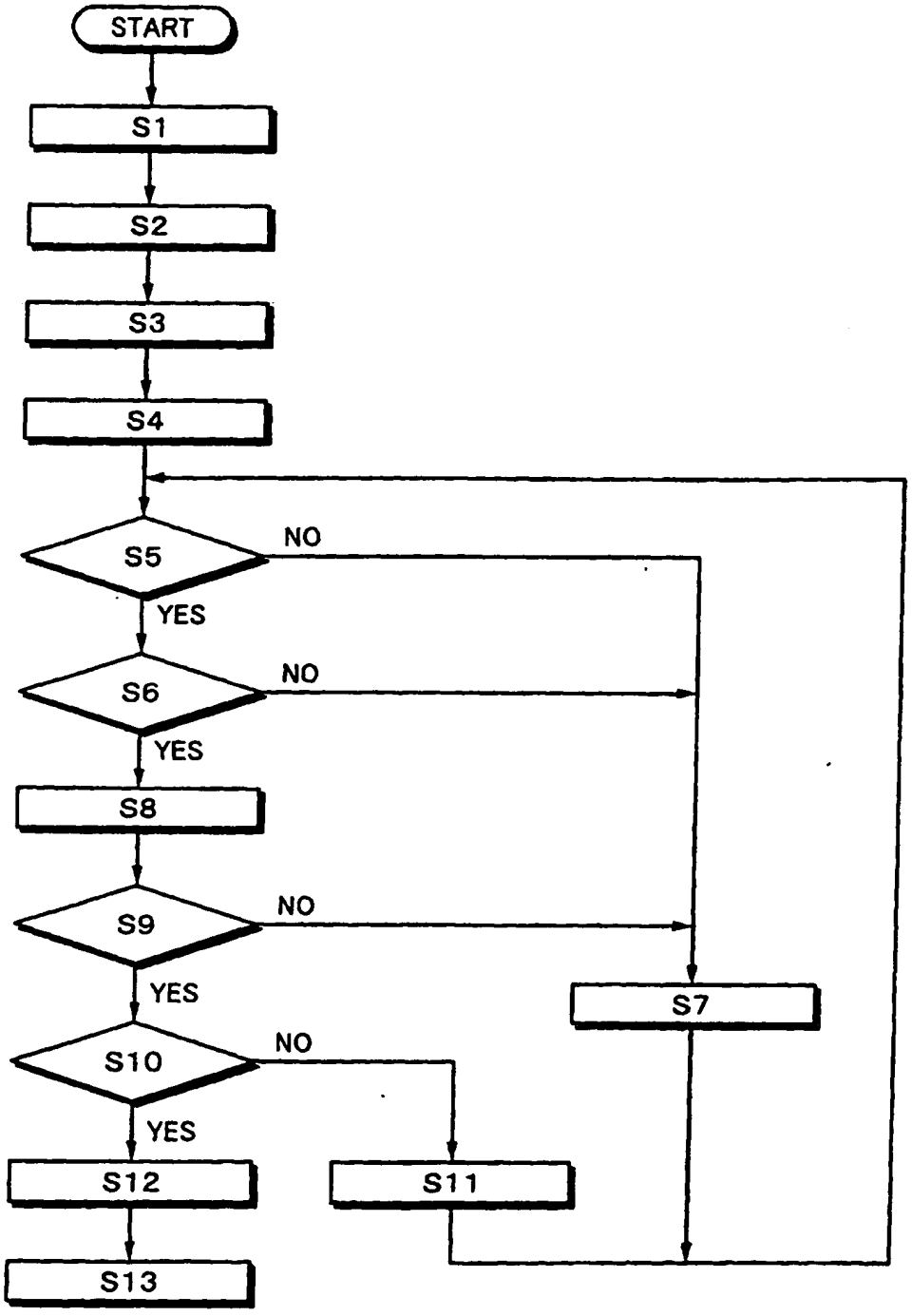

DSV+
DSV-
-50
-37
-63
-46
-54
-49
-51
(100) ARE SELECTED
(100) ARE SELECTED
L1
L2
t50
t51
t52
t53

Fig. 19


START
S1
S2
S3
S4
S5
NO
YES
S6
NO
YES
S8
S9
NO
YES
S7
S10
NO
YES
S12
S11
S13

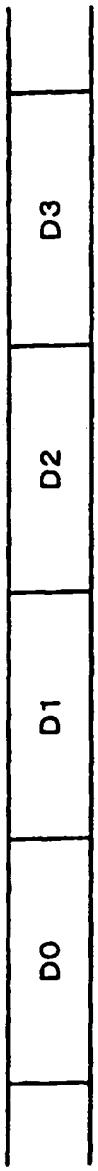


Fig. 20A

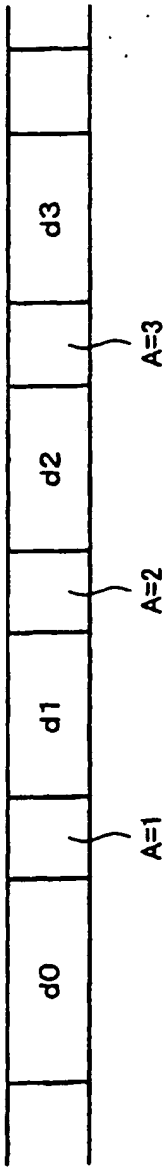


Fig. 20B

Fig. 21

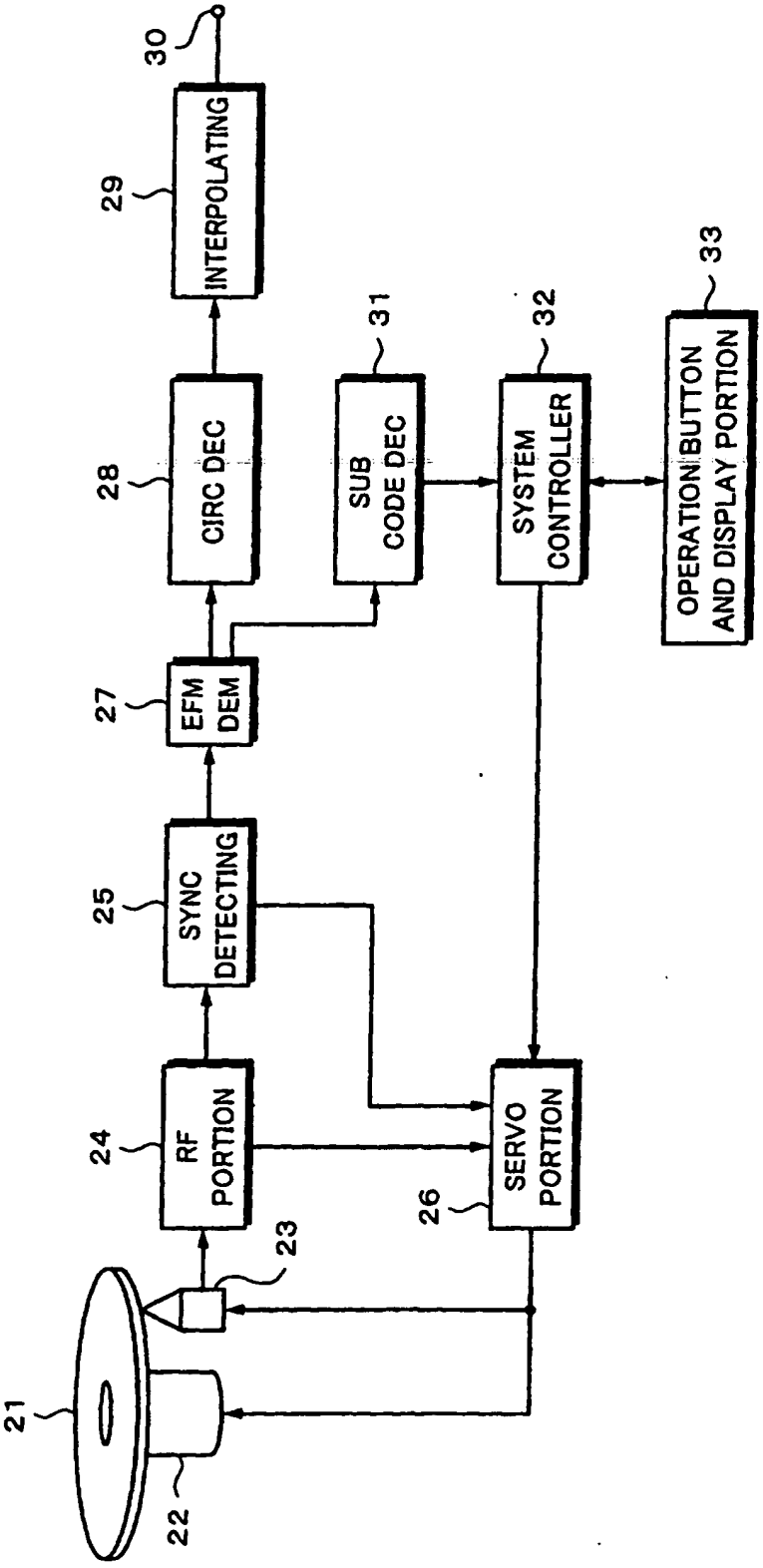
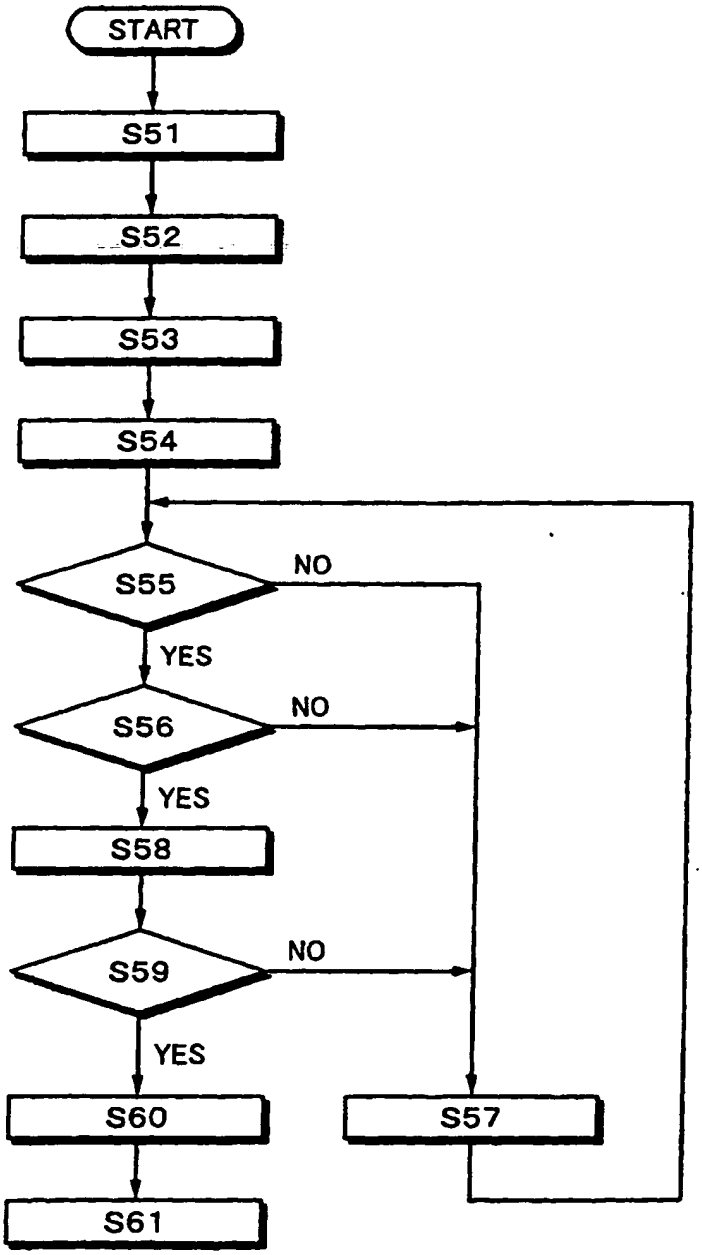

21
22
23
24
RF PORTION
25
SYNC DETECTING
26
SERVO PORTION
27
EFM DEM
28
CIRC DEC
29
INTERPOLATING
30
31
SUB CODE DEC
32
SYSTEM CONTROLLER
33
OPERATION BUTTON AND DISPLAY PORTION

Fig. 22


START
S51
S52
S53
S54
S55
NO
YES
S56
NO
YES
S58
S59
NO
YES
S60
S57
S61

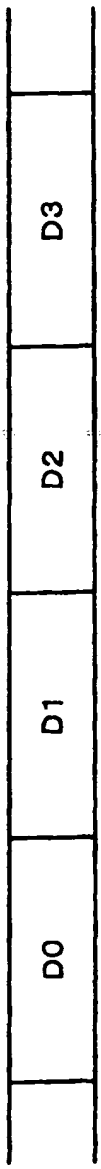
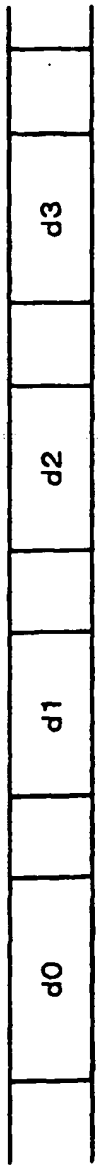


Fig. 23A



MP0=000
MP1=001
MP2=010
MP3=100

Fig. 23B

Fig. 24

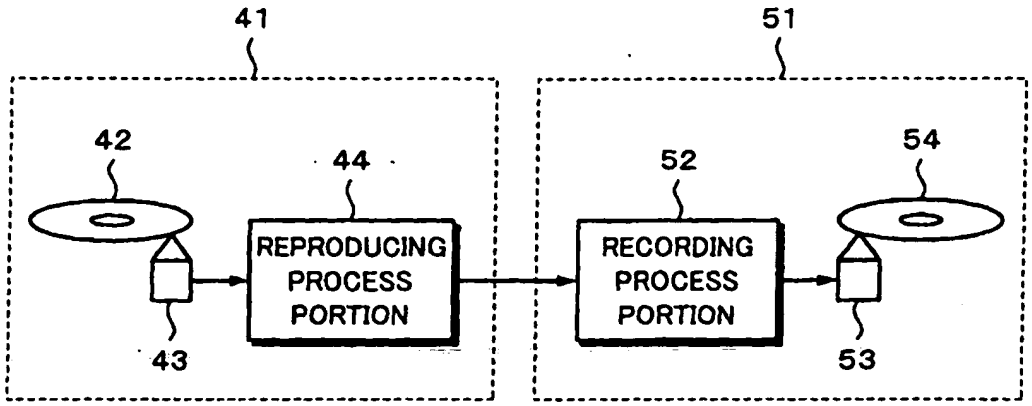


Fig. 25

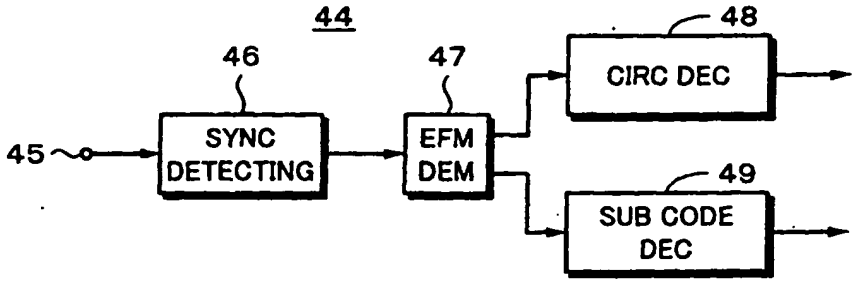
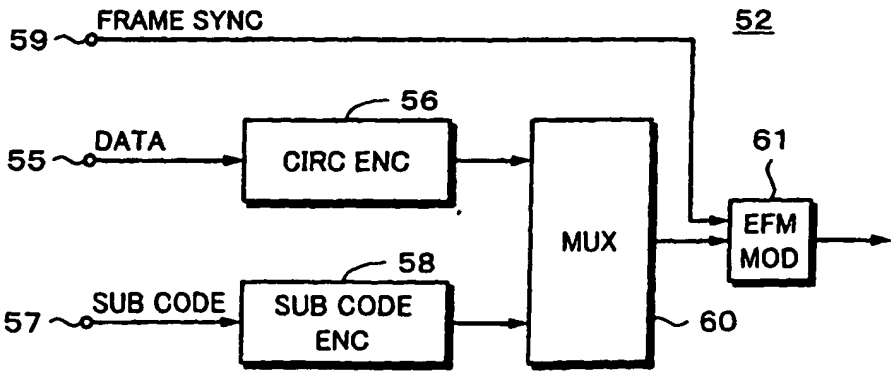


Fig. 26



DESCRIPTION OF REFERENCE NUMERALS

1	LASER LIGHT SOURCE
3	OPTICAL PICKUP
4	GLASS MASTER DISC
10	SUB CODE ENCODER
12	EFM MODULATOR
13	MULTIPLEXER
14	MERGING BIT SELECTING PORTION
15	DSV CONTROLLING PORTION
16	AREA CONTROLLING CIRCUIT
S1	INPUT DATA SYMBOLS D1 AND D2
S2	CONVERT DATA SYMBOLS D1 AND D2 INTO CODE SYMBOLS d1 AND d2, RESPECTIVELY
S3, S53	SELECT ALTERNATIVE MERGING BITS
S4	A1 = 0 n (A) = 0
S5, S55	Tmin = 3T ?
S6, S56	Tmax = 11T ?
S7	n (A) = n (A) + 1
S8, S58	STORE INFORMATION OF MERGING BITS THAT SATISFY CONDITIONS
S9	n (A) = 3 ?
S10	A = 2
S11	A = A + 1
S12, S60	CALCULATE DSV WITH STORED INFORMATION AND SELECT MINIMUM VALUE OF ABSOLUTE VALUES THEREOF

S13, S61	DECIDE MERGING BITS
S51	INPUT DATA SYMBOL D1
S52	CONVERT DATA SYMBOL D1 INTO CODE SYMBOL d1
S54	n = 0
S57	n = n + 1
S59	n = 3 ?

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP03/05876

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] G11B20/14, G11B20/10

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] G11B20/14, G11B20/10

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1922-1996	Jitsuyo Shinan Toroku Koho	1996-2003
Kokai Jitsuyo Shinan Koho	1971-2003	Toroku Jitsuyo Shinan Koho	1994-2003

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 7-245565 A (Sony Corp.), 19 September, 1995 (19.09.95), Full text; Figs. 1 to 13 (Family: none)	1-3,9-14, 19-24,29-34, 39-44
A	JP 62-281523 A (Matsushita Electric Industrial Co., Ltd.), 07 December, 1987 (07.12.87), Full text; Figs. 1 to 5 (Family: none)	1-48
A	JP 6-111486 A (Sony Corp.), 22 April, 1994 (22.04.94), Full text; Figs. 1 to 11 & EP 535560 A2	1-49

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 June, 2003 (12.06.03)	24 June, 2003 (24.06.03)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1998)